

Brittle 13.3

Intel Skylake-U (GT2)

REV : -1

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Brittle 13.3 Intel

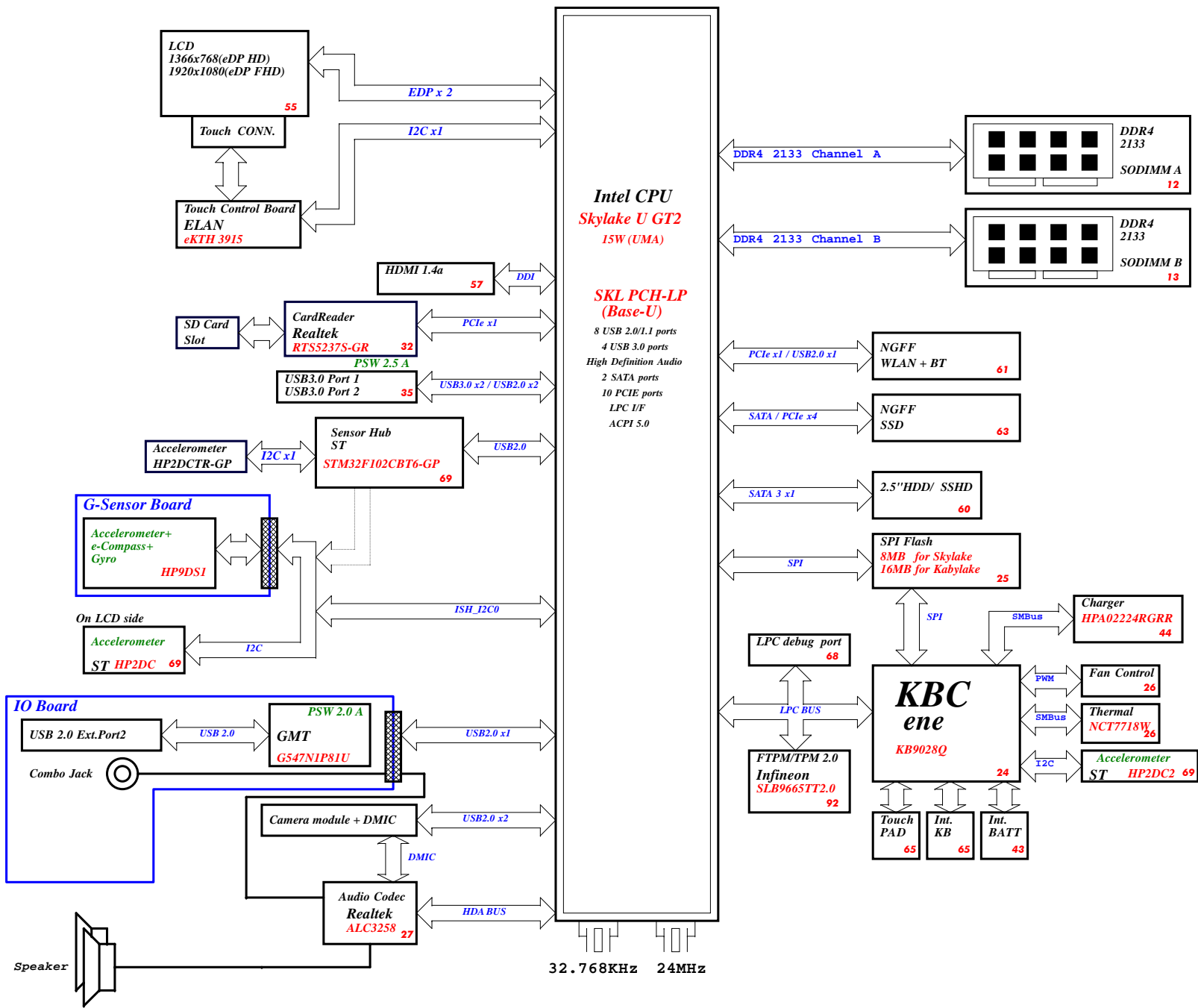
Rev
-1

Date: Thursday, February 18, 2016

Sheet 1 of 107

Project code:
4PD07M010001
PCB P/N: 15256-SD
Revision: -1

Brittle-Skylake U 13.3" Block Diagram

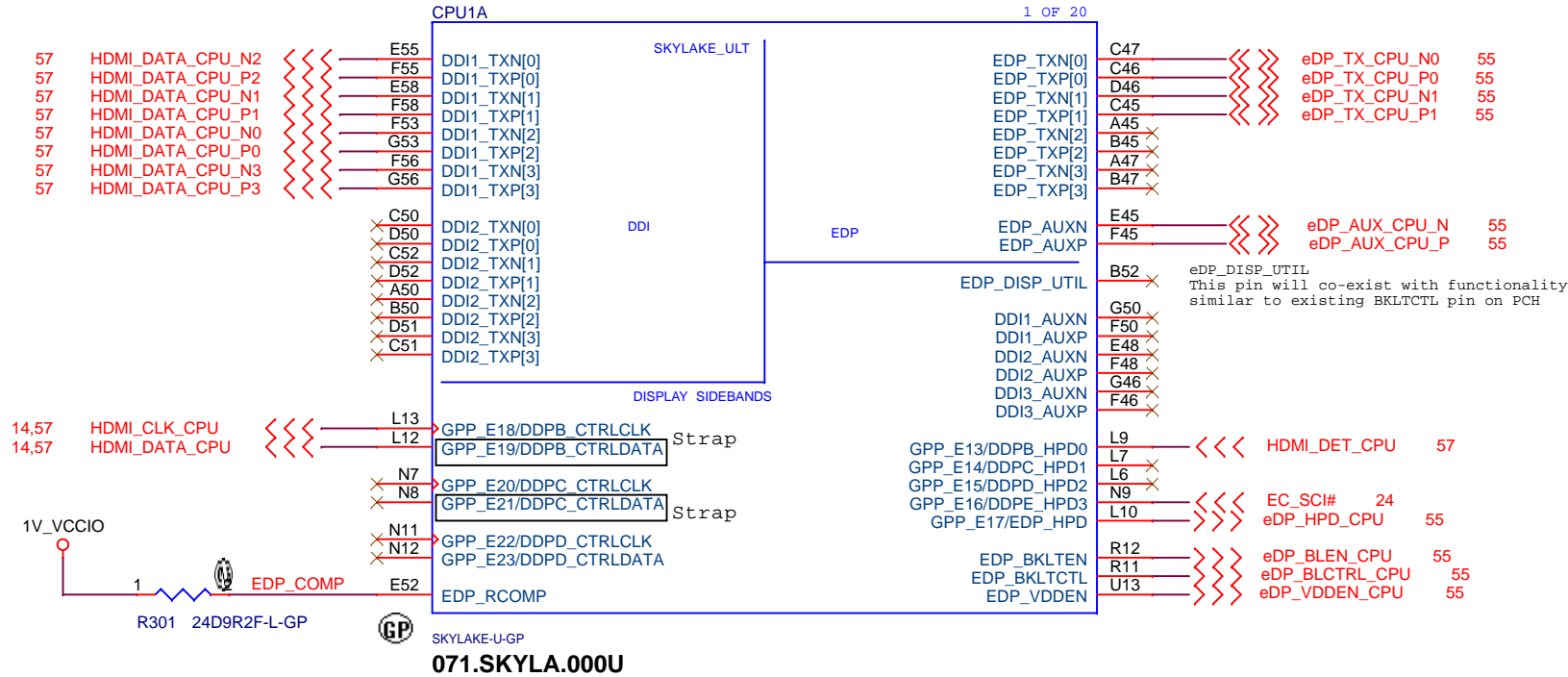


CHARGER	
HPA02224RGRR-1-GP 44	
INPUTS	OUTPUTS
AD+	19V_DCBATOUT
BT+	
SYSTEM DC/DC	
RT6575DQGW-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95859HRTZ-GP-U 46	
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE 1V_VCCGT 1V_VCCSA
DDR4	
RT8231AGQW-GP 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0 2D5V_S0
CPU PWR_1D0V	
AOZ1268QT-02-GP 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
CPU 1D8V_S5	
G9661-25ADJRE1U-GP 53	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
Switches	
40	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_DSW	3D3V_S0 3D3V_S5
1D0V_S5	1D0V_S3 1V_VCCIO
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Signal L7:GND L8:Bottom	

Main Func = CPU

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

HDMI



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ± 1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ± 1% Ω resistor

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ± 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ± 5% resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(DISPLAY)

Size

A4

Document Number

Brittle 13.3 Intel

Rev

-1

Date:

Thursday, February 18, 2016

Sheet

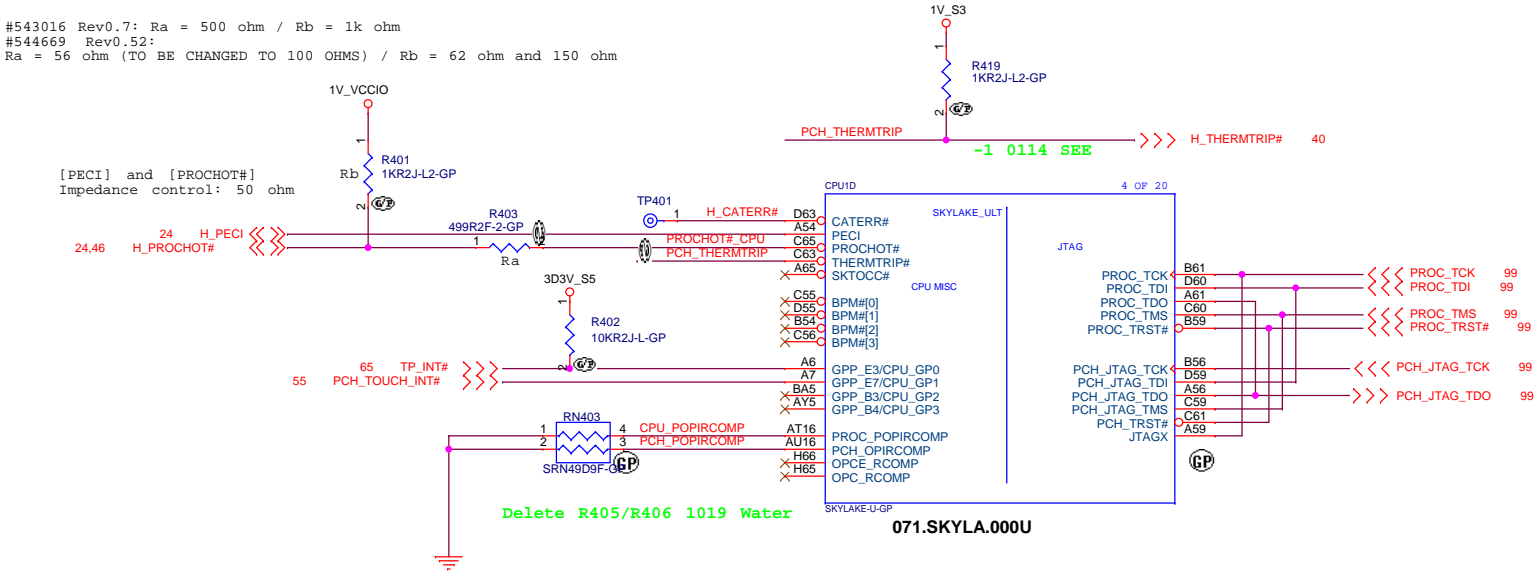
3

of

107

Main Func = CPU

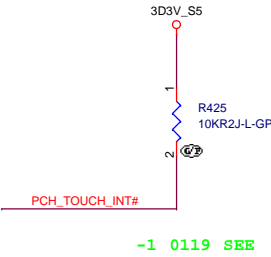
#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm



#543016 PDG Rev1.5 P.253

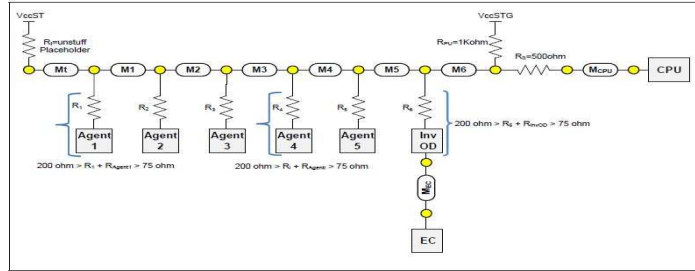
Table 10-2. Asynchronous and Sideband Legacy Signal Group

Signal Name	Description
PROCHOT#	PROCHOT# goes active when the Skylake processor temperature monitoring sensor(s) detects that the Skylake processor has reached its maximum safe operating temperature. This indicates that the Skylake processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the Skylake processor to activate the TCC.
CATERR#	This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The Skylake processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. On the Skylake processor, CATERR# is used for signaling the following types of errors: Legacy MCERRs - CATERR# is asserted for 16 BCLKs. Legacy IERRs - CATERR# remains asserted until warm or cold reset.
THERMTRIP#	Skylake processor output signal: Processor Asserted by the Skylake processor to indicate a thermal trip event, causing the Skylake processor to transition to an S5 state.



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



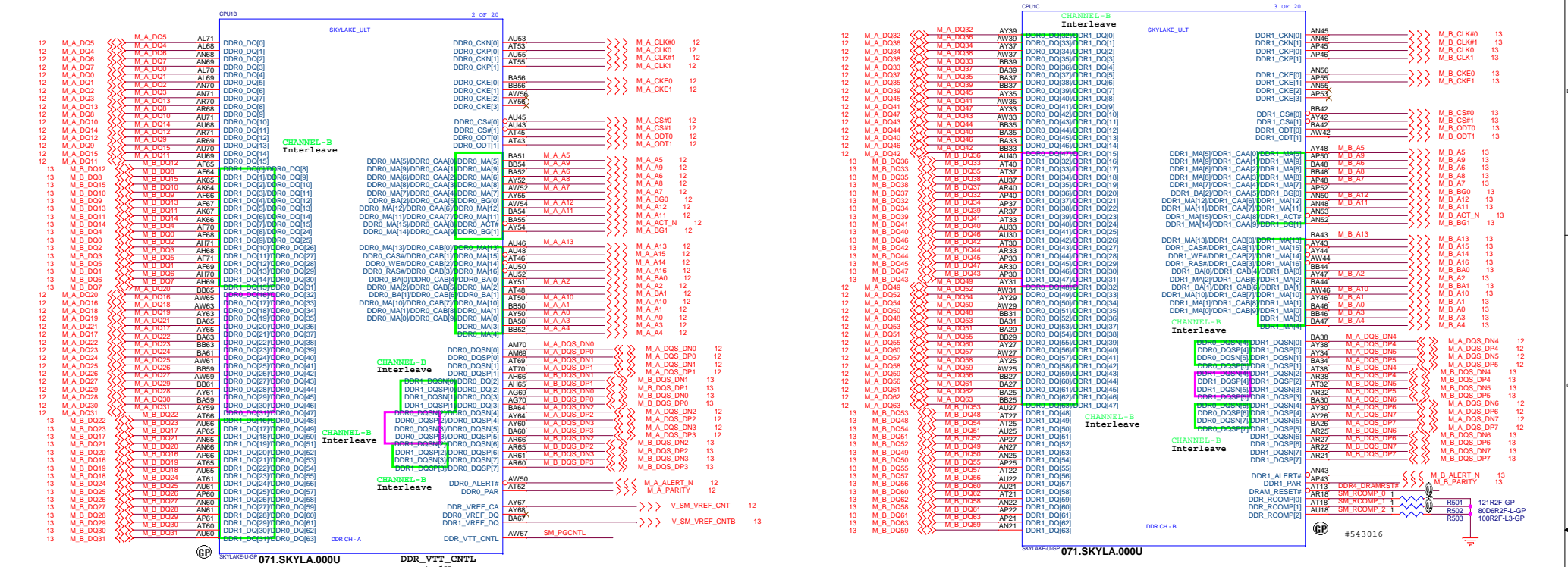
M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt: <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU_(JTAG/CPU SIDE BAND)		
Size A3	Document Number	Rev -1
Date: Thursday, February 18, 2016 Sheet 4 of 107		

Main Func = CPU

DDR4 ball type: Interleaved Type



#544924 EDS Rev0.95 P.122

Table 6-4

Signal Name	Description
DDR0_ACT#	Activation Command: ACT# HIGH along with CS# determines that the signals addresses below have command functionality.
DDR1_ACT#	
DDR2_ACT#	
DDR3_ACT#	
DDR4_ACT#	A16 use as RAS# signal
DDR5_ACT#	A15 use as CAS# signal
DDR6_ACT#	A14 use as WE# signal

SkyLake U Schematic CheckList

P.7 Table 59-7

DDR_VREF_CA	Connect to VREF_CA of Channel A (DDR0_XXX signals) DIMMs. Refer to the System Memory Interface Design Guideline Chapter in this Platform Design Guide.
DDR0_VREF_DQ	Not connected.
DDR1_VREF_DQ	Refer to the System Memory Interface Design Guideline Chapter in this Platform Design Guide.
DDR2_VREF_DQ	Connect to VREF_CA of Channel B (DDR1_XXX signals) DIMMs. Refer to the System Memory Interface Design Guideline Chapter in this Platform Design Guide.

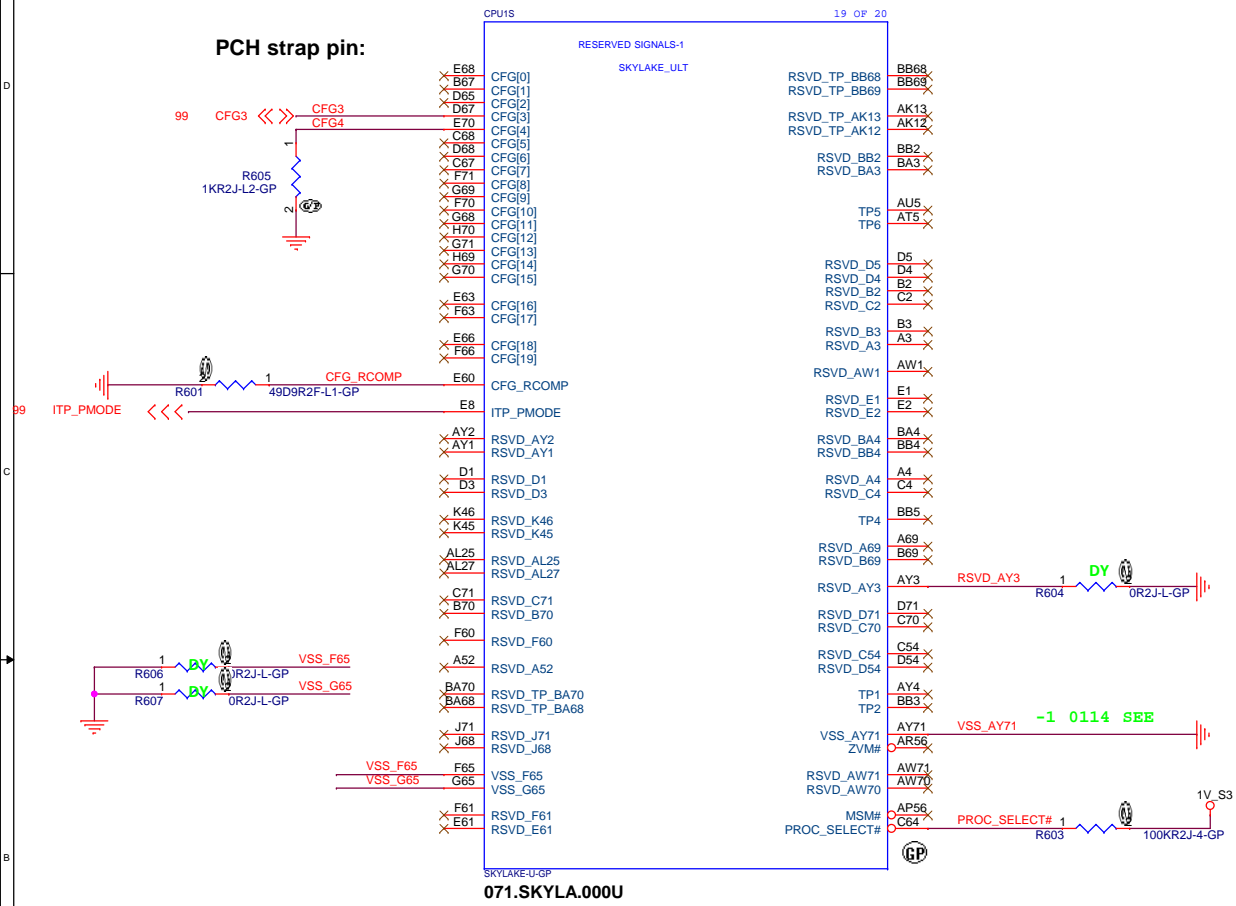
CKP and CKN differential signal swapping within a pair is not allowed.
DQ Bit Swapping is allowed within the same byte.
Byte Swapping is allowed within the same channel.
DQSP and DQSN differential signal swapping within a pair is not allowed.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei 10621, Taiwan, R.O.C.

File: CPU_(DDR)
Document Number: Brittle 13.3 Intel
Date: Thursday, February 18, 2016 Sheet 5 of 107

Main Func = CPU

#543016 EDS Rev0.95 P.124
Table 6-8



Description	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: 1 = (Default) Normal Operation; 0 = Stall.
	CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.
Availability	CFG[3]: Reserved configuration lane. CFG[4]: eDP enable: 1 = Disabled. 0 = Enabled.
	CFG[6:5]: PCI Express* Bifurcation 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training: 1 = (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training. CFG[19:8]: Reserved configuration lanes.

	Bonbon 15"	Rayleigh	fauchon 1.1
CFG[0]	1	1	1 (Reserved)
CFG[1]	1	1	1
CFG[2]	1	1	1
CFG[3]	1	1	1
CFG[4]	0	0	1
CFG[6:5]	1	1	1
CFG[7]	1	1	1
CFG[19:8]	1	1	1

(#544924 Rev0.95 P.124)

PROC_SELECT#	Processor Select: This pin is for compatibility with future platforms. It should be unconnected for SKL.
--------------	--

(#543016)

DISPLAY	PORT	PRESENCE	STRAP
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.		
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.		

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(RESERVED)

Size

A3

Document Number

Brittle 13.3 Intel

Date

Thursday, February 18, 2016

Sheet

6 of 107

Rev

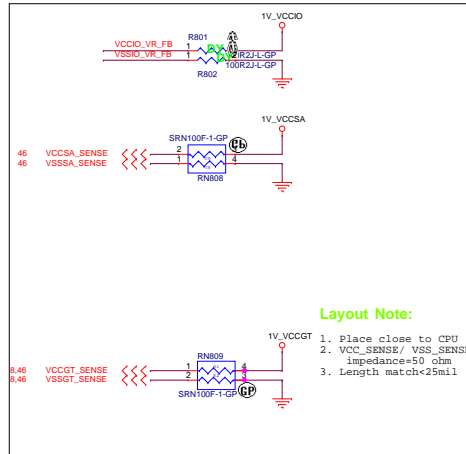
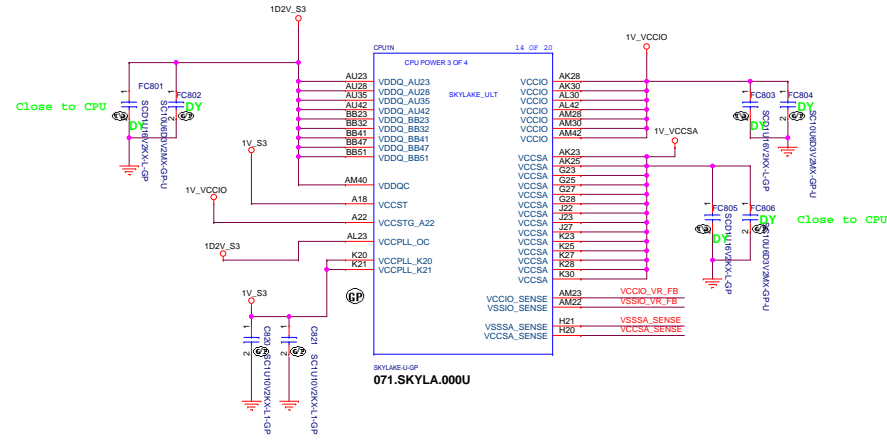
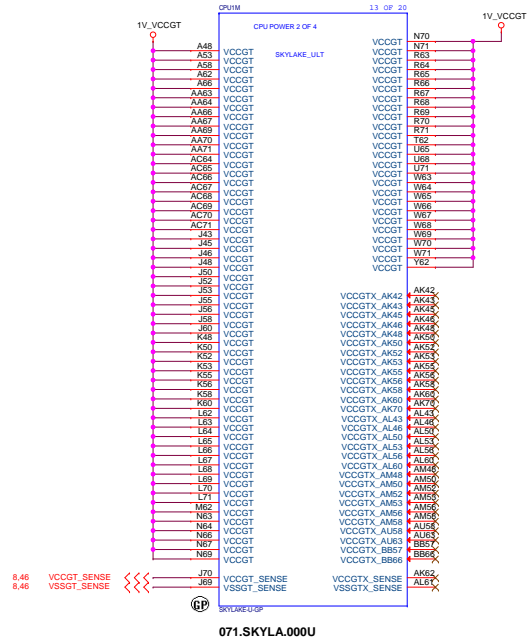
-1

543016 page663:

1U 0402 x 4

10U 0603 x 2

22U 0805 x 3

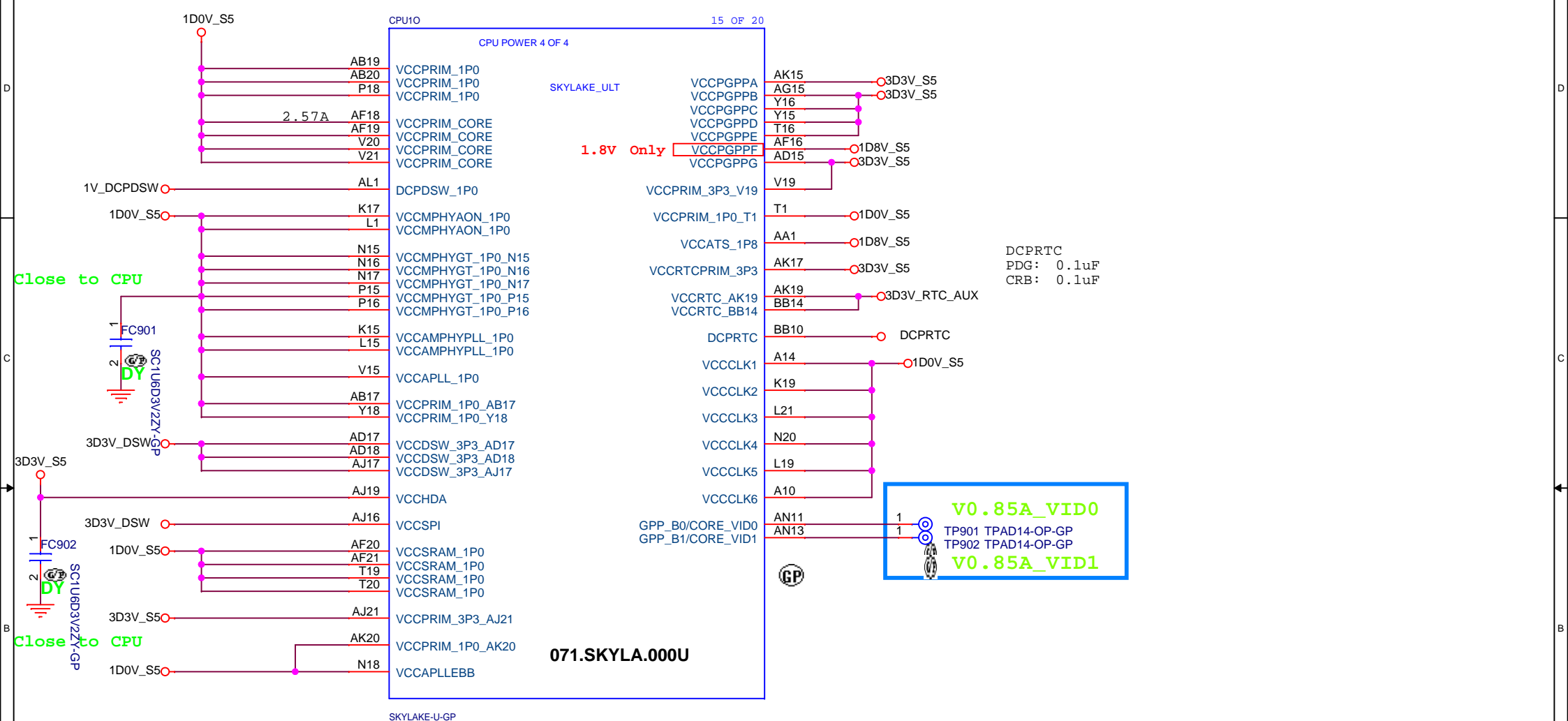


<Core Design>

緯創資通 Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
(Reserved)			
Size A2	Document	Number	Rev
		Brittle 13.3 Intel	-1
Date:	Thursday, February 16, 2016		Sheet 8 of 107

Main Func = PCH



<Core Design>

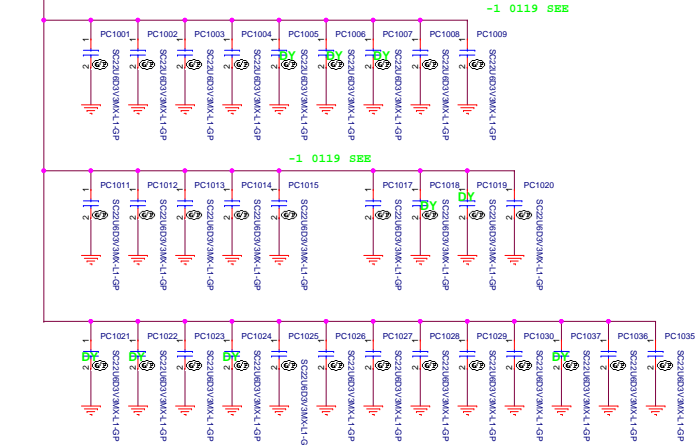
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU_(POWER1)		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016	Sheet 9	of 107

20150812 EVA modifr from 30 to 33 pcs

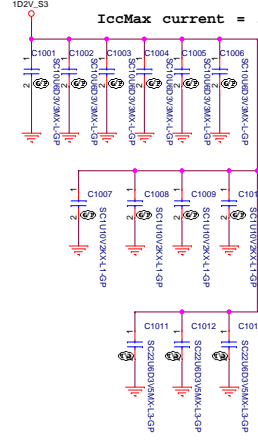
U-line 23e 28W
IccMax current-10ms max = 34 A

22U 0603 x 33

-1 0119 SEE



102V_S3 IccMax current = 3.5 A



VDDQ	2x 10 uF 0402 (Placeholder)	Place on secondary side, underneath the package
	4x 1 uF 0201 (Placeholder)	
	4x 10 uF 0402	Place as close to the package as possible
	3 x 22 uF 0603	Place as close to the package as possible

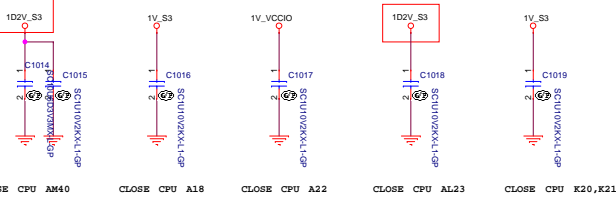
20150806 Cloud follow Anne

IccMax = 0.04 A

IccMax = 0.04 A

IccMax = 0.26 A

IccMax = 0.12 A



VCCIO

1U 0402 x 8

+VCCIO (IccMax. = 2.73A)

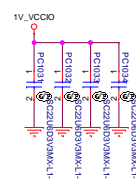


Table 52-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
Vcc Power Plane at VR output	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
VccGT Power Plane at VR output	1x 220 uF (@4.5mO ESR)	Placed at backside side near to VR output
VccGT Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
VccGT Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output. Additional components needed when supporting 23e
VccGTx Power Plane at VR output	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output. Only needed when supporting 23e
VccIO Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VccSA Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
Note: VccGTx decoupling is only required for SKL U 2+3 (GT3).

Table 52-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	9x 22 uF 0603		Place on secondary side, underneath the package
	7x 10 uF 0402		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
	35x 1 uF 0201		
		8x 47 uF 0805 (6.3V) ¹	Place as close to the package as possible
		8x 10 uF 0402	
VccGT	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0201		
		5x 47 uF 0805 (6.3V) ¹	Place as close to the package as possible
		7x 22 uF 0603	
		3x 47 uF 0805	Place as close to the package as possible
		5x 22 uF 0603	Additional components needed when supporting 23e
		10x 10 uF 0402 (Placeholder)	Place as close to the package as possible
VccGTx	20x 10 uF 0402 (Placeholder)		Place on secondary side, underneath the package
	20x 1 uF 0201 (Placeholder)		
		8x 10 uF 0402	Place on secondary side, underneath the package
VccGTx	8x 10 uF 0402		Place on secondary side, underneath the package. Only needed when supporting 23e
		8x 22 uF 0603	Only needed when supporting 23e

Table 52-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
VccSA	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0201		
VccIO		6x 10 uF 0402	Place as close to the package as possible
	2x 10 uF 0402 (Placeholder)		Place on secondary side, underneath the package
VDDQ	4x 1 uF 0201 (Placeholder)		
		4x 1 uF 0402	Place as close to the package as possible
		4x 10 uF 0402	Place as close to the package as possible
VDDQC	1x 1 uF 0201 (Placeholder)	3 x 22 uF 0603	Place as close to the package as possible
			Place on secondary side, underneath the package
VccPLL		1 x 10 uF 0402	Place as close to the package as possible
VccPLL_OC		1x 1 uF 0402	Place as close to the package as possible
VccST		1x 1 uF 0201	Place as close to the package as possible
VccSTG		1x 1 uF 0402 (Placeholder)	Place on secondary side, underneath the package. Placeholder only
VccOEPIO		2x 10 uF 0402	Place on secondary side, underneath the package
VccORC		1x 10 uF 0402	Place on secondary side, underneath the package
		6x 1 uF 0201	

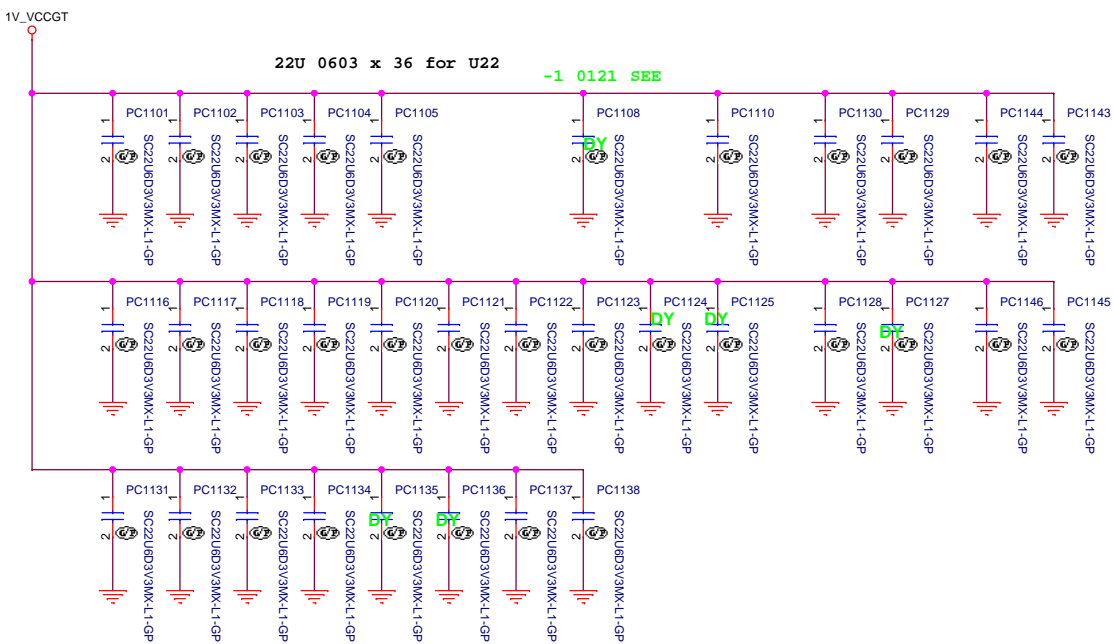
	Bonbon 15" GT3e	Bonbon 15" GT2	Fachon 13"
CPU CORE	22U 0603 x30 330U x2	22U 0603 x30 330U x2	22U 0805 x24 330U x1
VCCSA	22U 0603 x 5 22U 0603 x 5(DY)	22U 0603 x 5 22U 0603 x 5(DY)	22U 0603 x 8
VCCGT	22U 0603 x 32 330U x2	22U 0603 x 32 330U x1	22U 0805 x 23 22U 0603 x6 330U x1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipai Hsien 301, Taiwan, R.O.C.

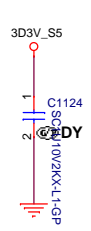
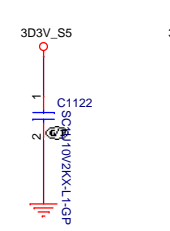
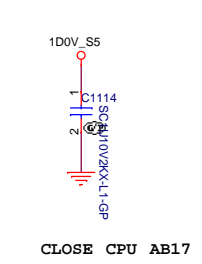
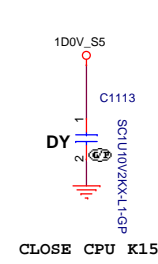
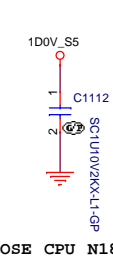
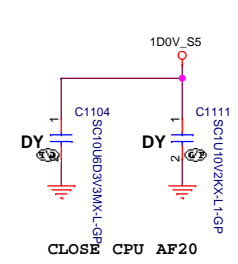
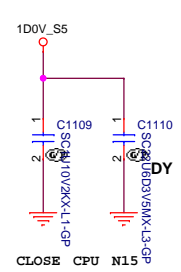
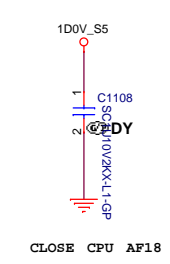
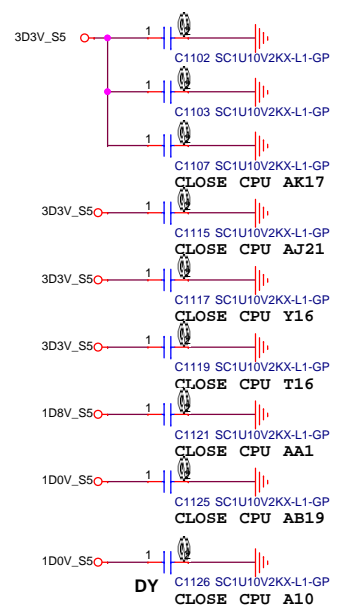
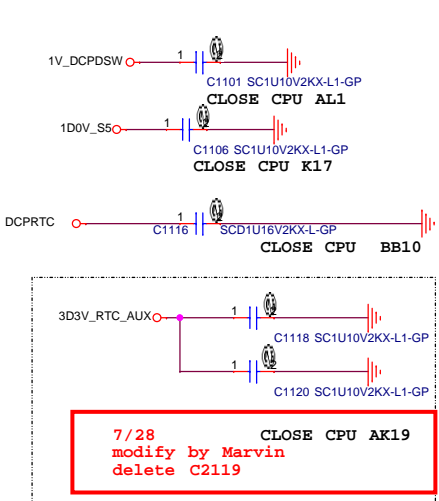
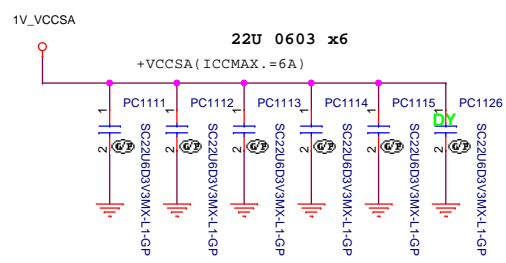
CPU_(Power CAP1)		
Size A2	Document Number	Rev -1
Brittle 13.3 Intel		
Date: Thursday, February 16, 2016	Sheet 10	of 107

Main Func = CPU

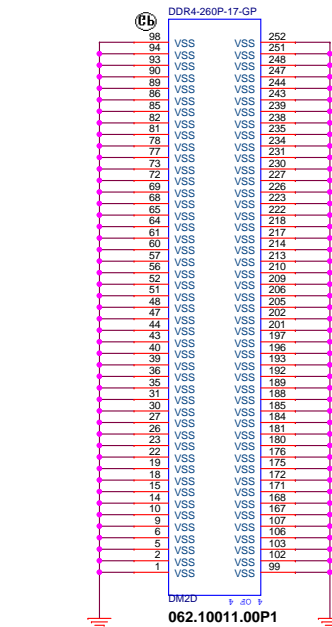
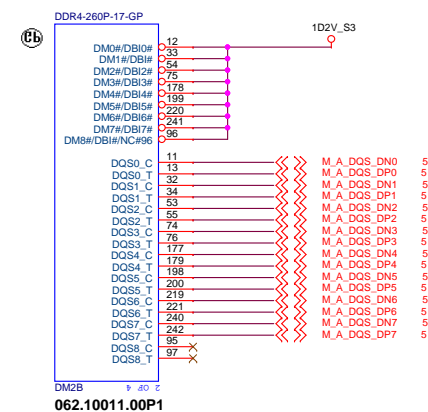
SLICED GT



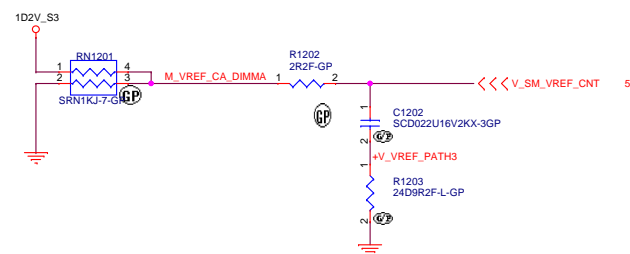
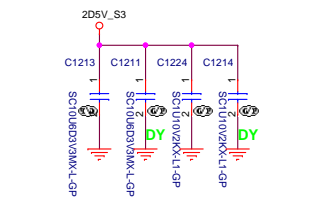
VCCSA 20150812 EVA modify to 6 pcs



Standard Type

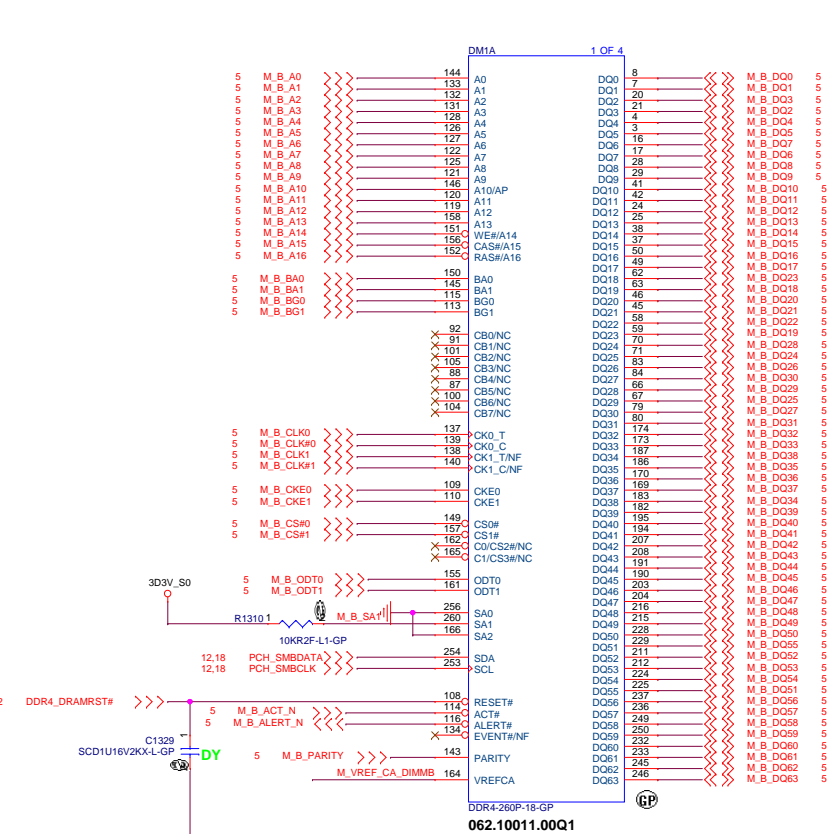


SPD SA2	0
SPD SA1	0
SPD SA0	0

[illegible]

Main Func = DDR SODIMM

Reverse Type

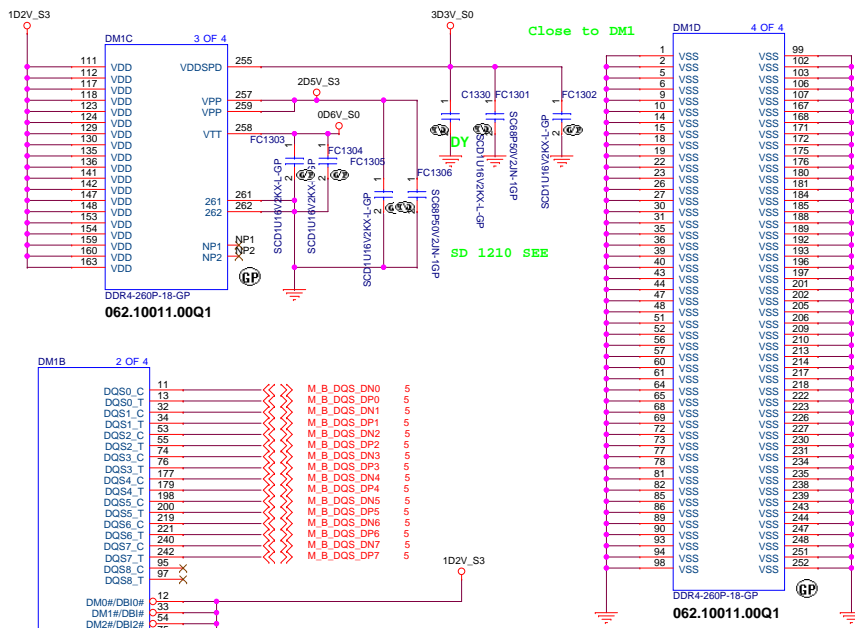
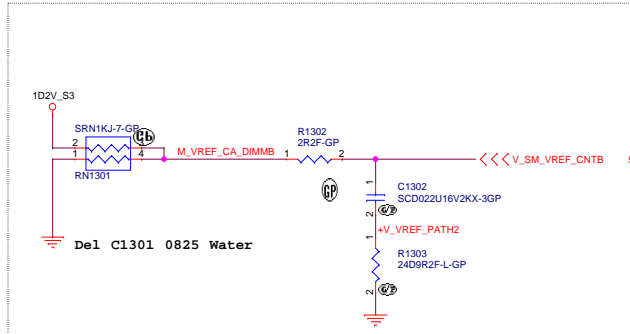


Layout Note :
VREFCA traces should
have width=20 mil;
spacing=20 mil

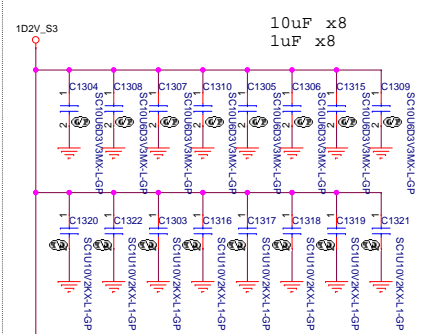
SPD Address of DIMMB

SPD SA2	0
SPD SA1	1
SPD SA0	0

SA_DIMM_VREFDQ



Layout Note :
Place these Caps near DIM1

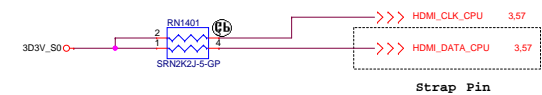


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsichin,
Taipei, Hsin 221, Taiwan, R.O.C.

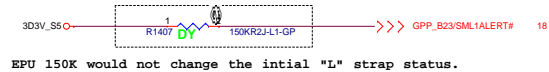
Title			DDR4-SODIM CHANNEL B
Size	Document	Number	Brittle 13.3 Intel
Custom			
Date:	Thursday, February 18, 2016	Sheet	13 of 107

CPU PCH Strap Pin



3D3V_S0 Domain

Status	IPD/IPU	Signal	Strap Fun.	1	0
0	IPD	SPKR /GPP_B14	Top Swap Override	Enable	Disable
0	IPD	GSPIO_MOSI/ GPP_B18	No Reboot	Enable	Disable
0	IPD	GSPII_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	LPC	SPI
1	IPD	DDPB_CTRLDATA /GPP_E19	Display Port B Detected	Detected	Not detected



3D3V_S5 Domain

Status	IPD/IPU	Signal	Strap Fun.	1	0
0	IPD	SMBALERT# /GPP_C2	TLS Confidentiality	Enable	Disable
0	IPD	SML0ALERT# /GPP_C5	eSPI or LPC	eSPI	LPC
0	IPD	SML1ALERT# /PCHHOT# /GPP_B23	Reserved	no description	no description

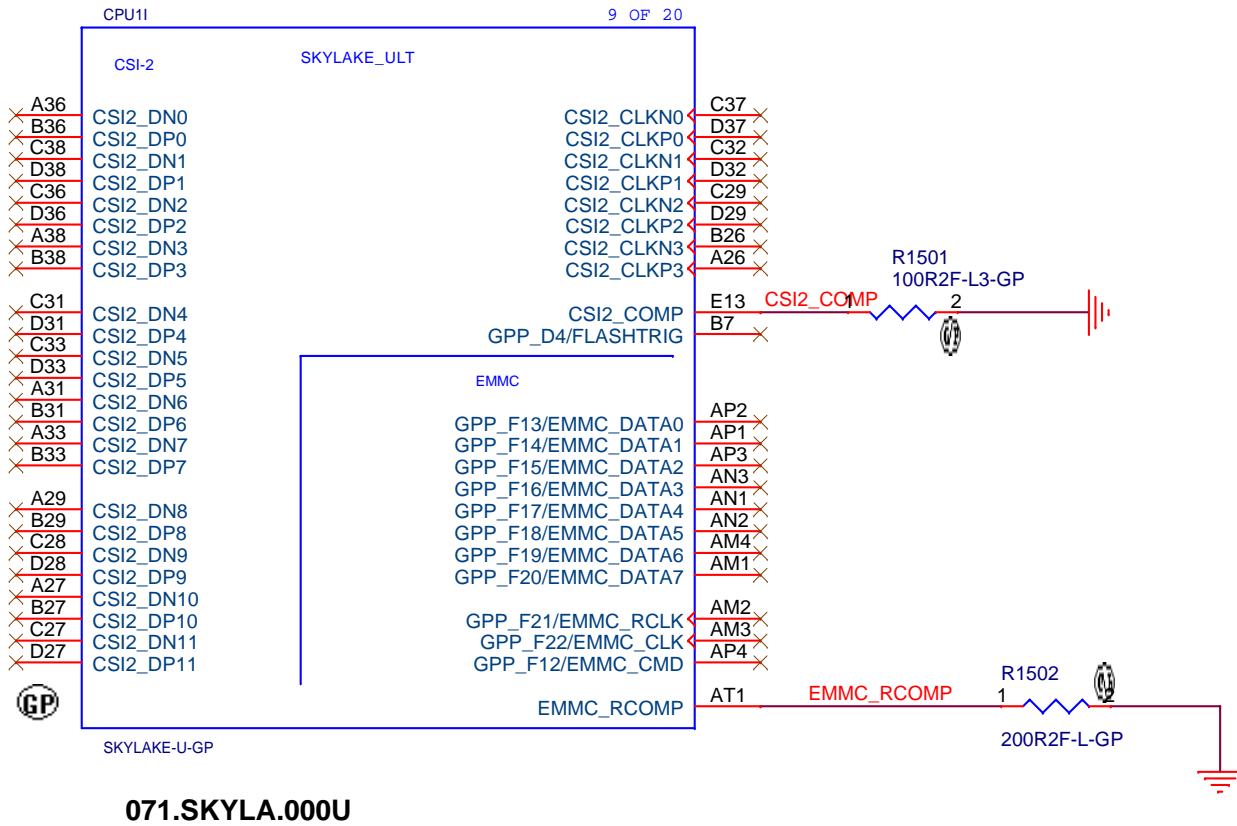
3D3V_VCCSPI Domain

Status	IPD/IPU	Signal	Strap Fun.	1	0
1	IPU	SPI0_IO2	Reserved	no description	no description
1	IPU	SPI0_IO3	Reserved	no description	no description

Reserved

Status	IPD/IPU	Signal	Strap Fun.	1	0
1	IPU	SPI0_MOSI	Reserved	no description	no description
1	IPU	SPI0_MISO	Reserved	no description	no description
0	IPD	HDA_SDO /I2S_TXD0	Flash Descriptor Security Override	Disable	Enable
0	IPD	DDPC_CTRLDATA /GPP_E21	Display Port C Detected	detected	not detected

Main Func = PCH



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(CS-2/EMMC)Size
A

Document Number

Brittle 13.3 Intel

Rev
-1

Date: Thursday, February 18, 2016

Sheet 15 of 107

Main Func = PCH

#543016 Rev1.5 P.296

Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints: Required to refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

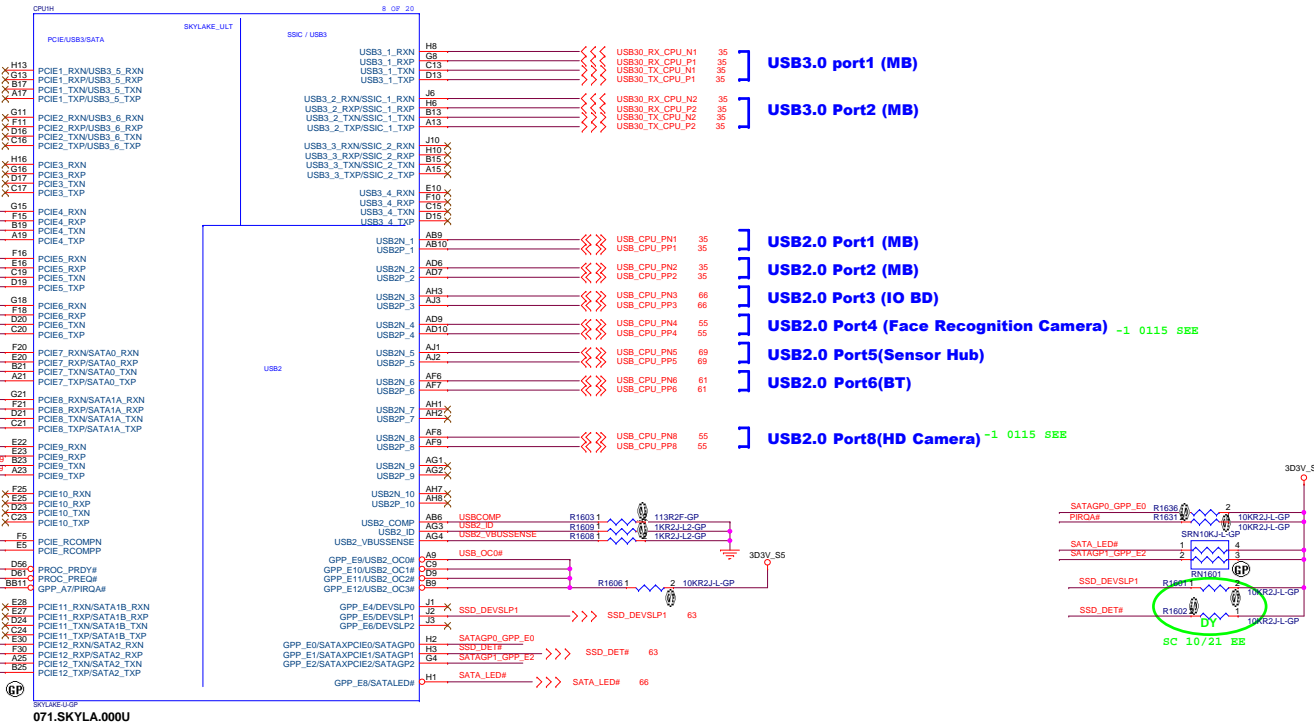
WLAN

SSD (PCIe)

SSD (SATA)

Cardreader

HDD



(#543016) When used as DEVS_LP, no external pull-up or pull-down termination required from SATA Host DEVS_LP.

PCIe Table

Port	Device	Share BUS
1	N/A	
2	N/A	
3	N/A	
4	WLAN	
5-7	SSD (PCIe)	
8	SATA	
9	Cardreader	
12	HDD	

USB 2.0 Table

Pair	Device
0	USB3.0 Port 1
1	USB3.0 Port 2
2	USB2.0 Port 3
3	CDD Port 4/8
4	WLAN(Bluetooth) Port 6
5	Sensor Hub Port 5

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3.3.
(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 kΩ to 10 kΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

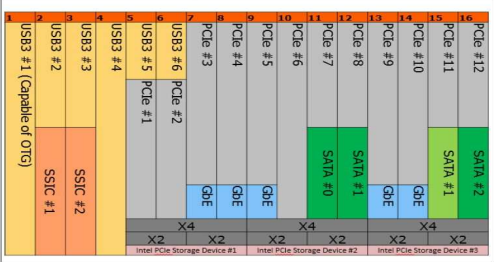
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes												
		1	2	3	4	5	6	7	8	9	10	11	12	
U	1x4	Port1			Port5				Port9					
	2x2	Port1		Port3		Port5		Port7		Port9			Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12	
Y	1x4	Port1			Port5									
	2x2	Port1		Port3		Port5		Port7						
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8					
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8					
	1x2									Port9				
	2x1									Port9		Port10		

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)



(#545659 Rev0.7 P.207,208)

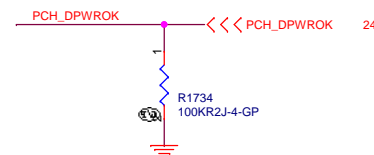
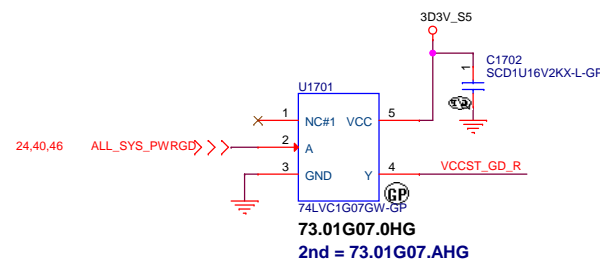
SATAGP0/ GPP_E0/ SATAPXIC0	I	Serial ATA Port [0] General Purpose Inputs: When configured as SATAGP_0, this is an input pin that is used as an interlock switch status indicator for SATA Port 0. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. Note: The default use of this pin is GPP_E0.
SATAGP1/ GPP_E1/ SATAPXIC1	I	Serial ATA Port [1] General Purpose Inputs: When configured as SATAGP_1, this is an input pin that is used as an interlock switch status indicator for SATA Port 1. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. Note: This default use of this pin is GPP_E1.
SATAGP2/ GPP_E2/ SATAPXIC2	I	Serial ATA Port [2] General Purpose Inputs: When configured as SATAGP_2, this is an input pin that is used as an interlock switch status indicator for SATA Port 2. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. Note: The default use of this pin is GPP_E2.

Integrated Pull-ups and Pull-downs

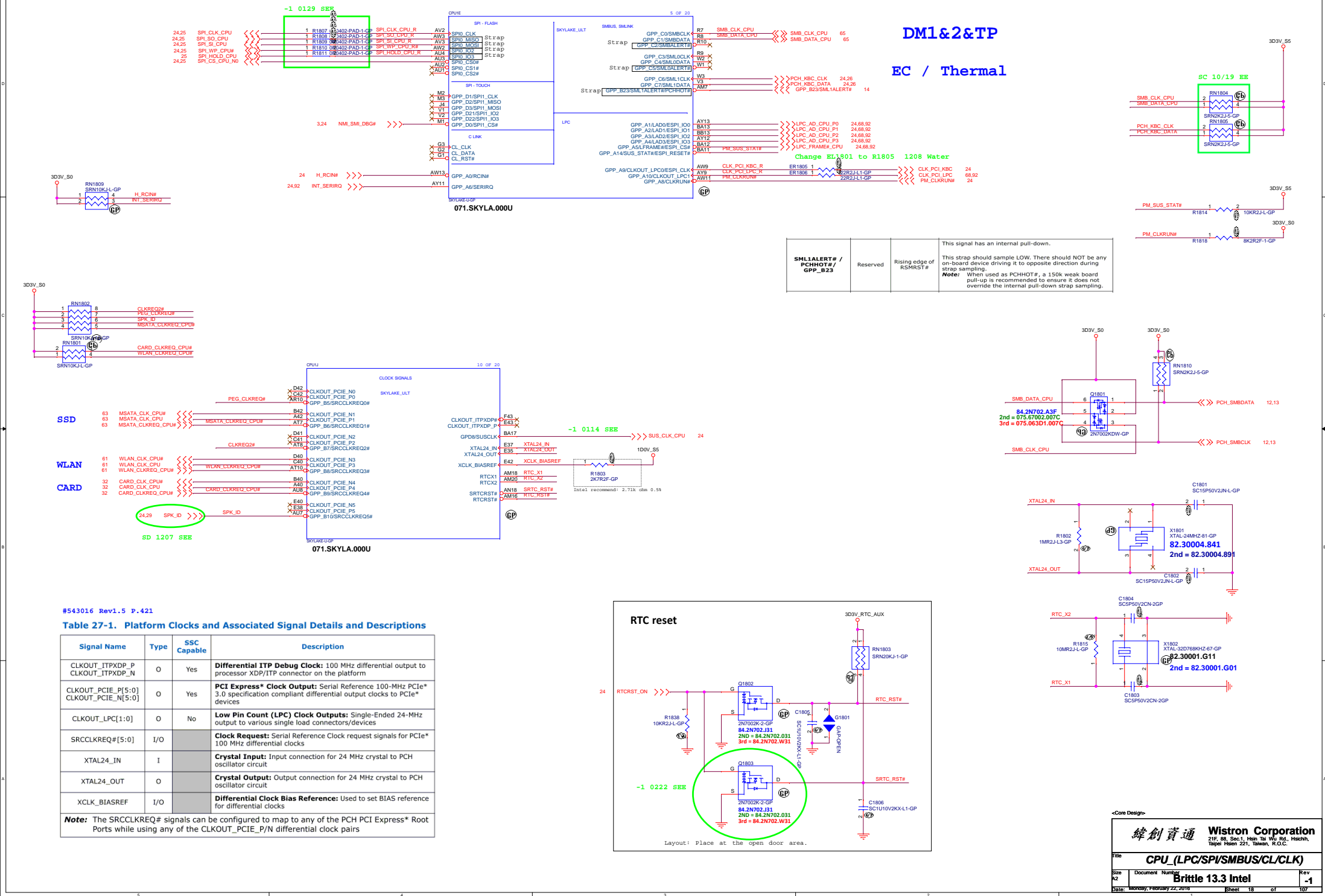
Signal	Resistor Type	Nominal Value	Notes
SATAGP1[0]/GPP_E[1:0] SATAGP2[0]/GPP_E[2:0]	Pull-up	20 kΩ	1, 2
Note: 1. SATAGP[2:0]/GPP_E[2:0] and SATAGP[5:3]/GPP_E[2:0] has two native functions – the first native function (SATAPX, PCIe* _{LP} L1) is selected if the Pin L10 soft-sense SATAPX_PCIE* _{LP} MODE = 11b. Setting SATAPX_PCIE* _{LP} MODE = 11b also enables an internal pull-up resistor in this pin to allow flexible I/O selection of SATA Port x or PCIe Port x to be done based on the type of card installed (if sampled value = 3, select SATA; if sampled value = 0, select PCIe*). SATAPX_PCIE* _{LP} Select GPIO polarity for SATA Port x (SFGPA) and Soft strobe are handled through FITC and described in SkyLake Processor SPI Flash Programming Guide (CDI doc #TBD). 2. Simulation data shows that these resistor values can range from 14 kΩ – 26 kΩ.			

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 301, Taiwan, R.O.C.

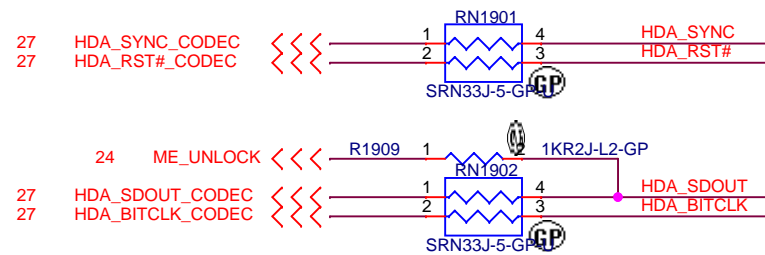
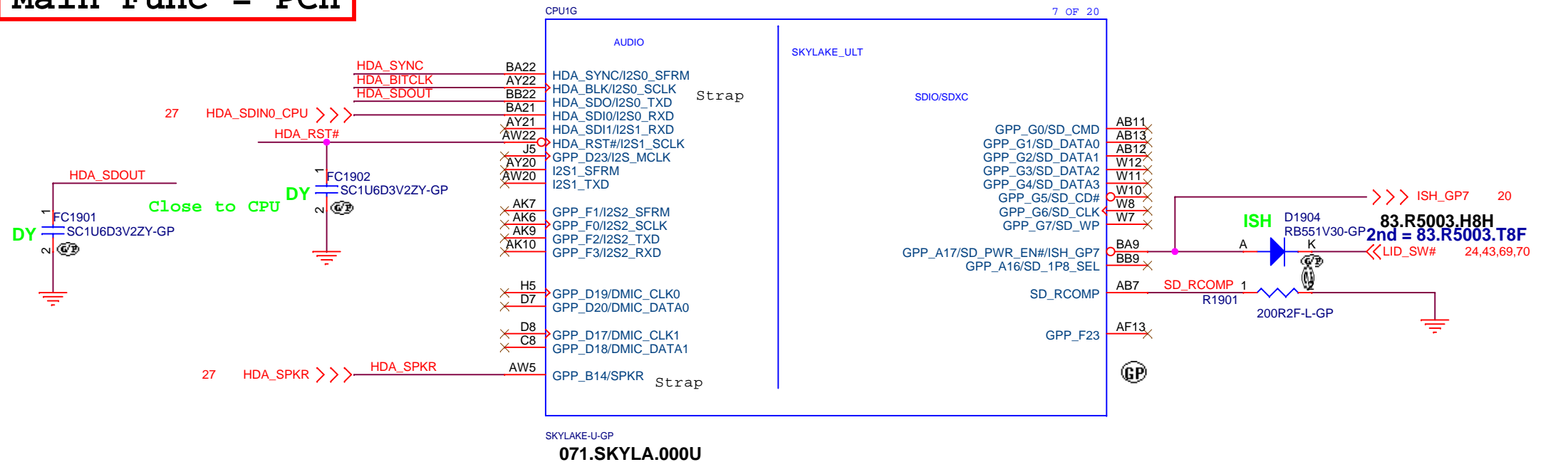
File: CPU_ (PCIe/SATA/USB)
Size: Document Number: Brittle 13.3 Intel
Date: Thursday, February 16, 2016 Sheet: 16 of 107



The diagram illustrates a 1-wire bus topology. It starts with a **Driver** block connected to a series of components. The components are connected in sequence: **M1**, **M2**, a pull-up resistor R_{PU} (labeled $1K\Omega$) connected to V_{CCST} , a series resistor R_S (labeled 60Ω), M_{CPU} , and finally the **CPU** block. Yellow circles indicate the connection points between these components.



Main Func = PCH



<Core Design>

緯創資通

Wistron Corporation

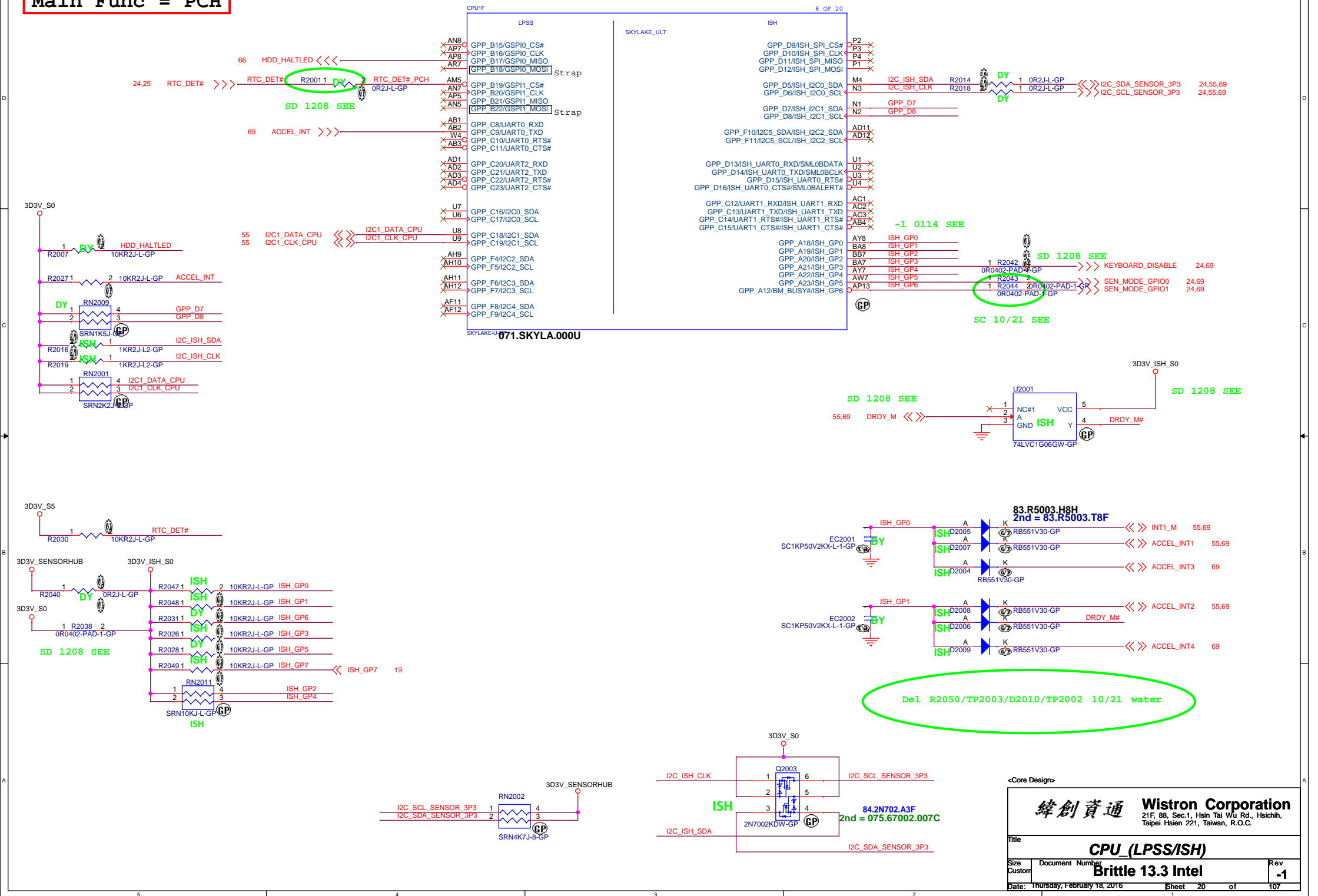
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>CPU_(AUDIO/SDIO/SDXC)</i>
-------	-------------------------------------

Size A4	Document Number Brittle 13.3 Intel	Rev -1
------------	--	------------------

Date: Thursday, February 18, 2016 Sheet 19 of 107

Main Func = PCH



(Blanking)

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(CS-2/EMMC)

Size

Document Number

Rev

A3

Brittle 13.3 Intel

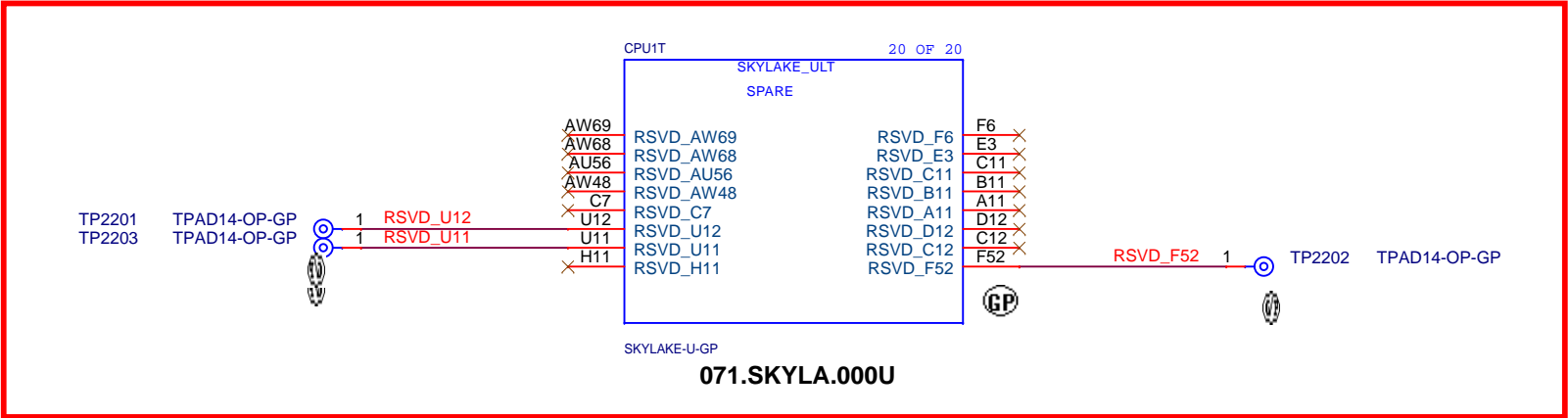
-1

Date: Thursday, February 18, 2016

Sheet 21 of 107

1

Main Func = PCH



7/28
modify by Marvin
reserved test point

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU_(RSVD)		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016		Sheet 22 of 107

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(VSS)

Size
A3

Document Number

Number **Brittle 13.3 Intel**

Rev

-1

Date: Thursday, February 18, 2016

Sheet 23 of 107

SSID = KBC

KBC9028Q

HP Limit Signal Detect

PCB VERSION

Pull Voltage Register	Pull-Low Register	Pull-High Register	Typical Voltage
SA	100.0 K	10.0 K	3.000 V
SB	100.0 K	20.0 K	2.750 V
SC	100.0 K	33.0 K	2.481 V
SD	100.0 K	47.0 K	2.245 V
* -1	100.0 K	64.9 K	2.001 V
-2	100.0 K	76.8 K	1.867 V
-3	100.0 K	100.0 K	1.850 V
-4	100.0 K	143.0 K	1.358 V
-5	100.0 K	174.0 K	1.204 V

MODEL ID

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	Model ID EC RAM
Nougat SKL-U	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	0x31
Nougat KBL-U	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V < 2.875 V	0x41
Brittle SKL-U	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V < 2.616 V	0x32
Brittle KBL-U	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V < 2.363 V	0x42
Marshmallow SKL-U	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V < 2.123 V	0x33
Marshmallow KBL-U	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V < 1.934 V	0x43

Wistron Corporation

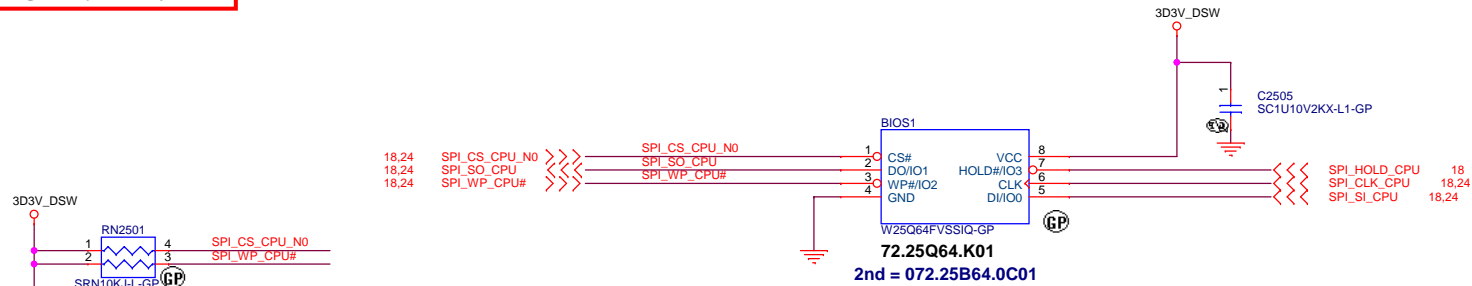
21F, 6B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

File: **KBC NPCE285PA0DX-GP**

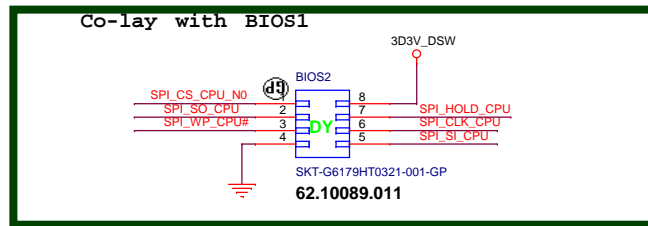
Size: **84.73906.E11**

Date: Tuesday, February 16, 2016 Sheet: 24 of 107

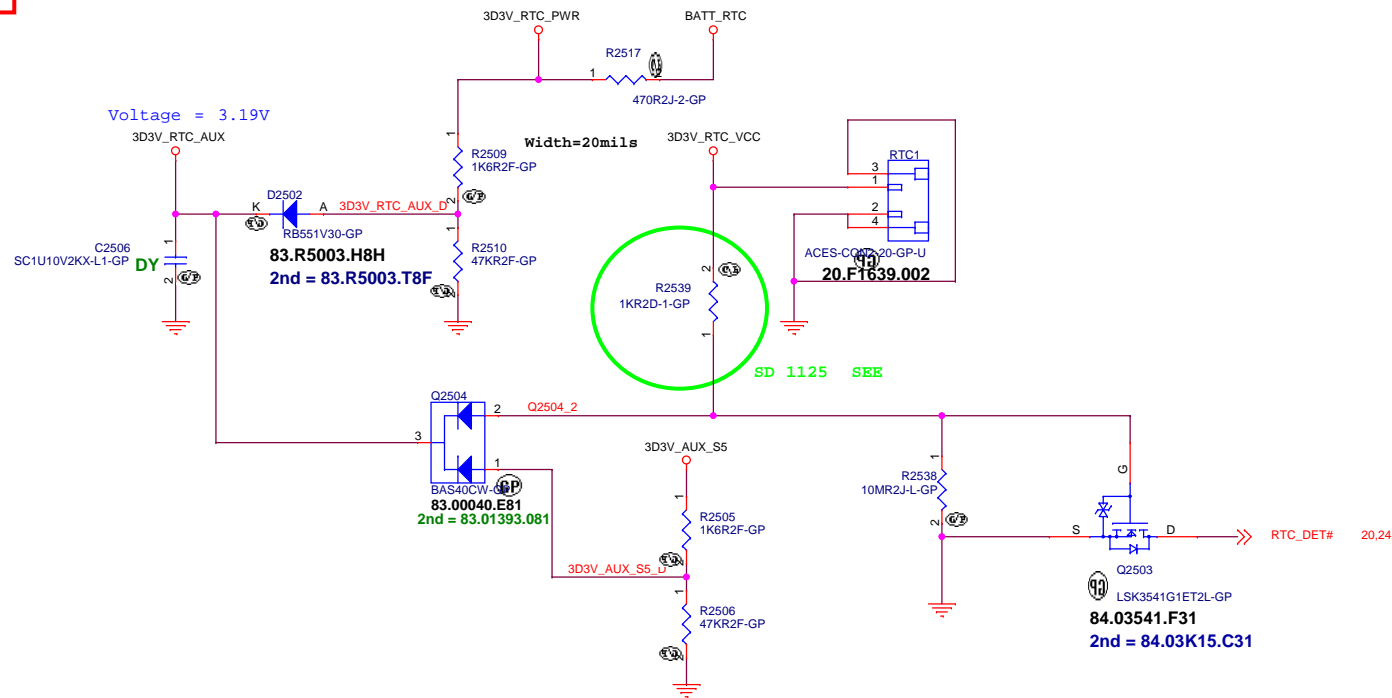
SSID = Flash.ROM



SPI FLASH ROM 16M byte



SSID = RBAT



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash(KBC+PCH)/RTC

Size

Document Number

Brittle 13.3 Intel

Date: Thursday, February 18, 2016

Sheet 25 of 107

Rev	
-----	--

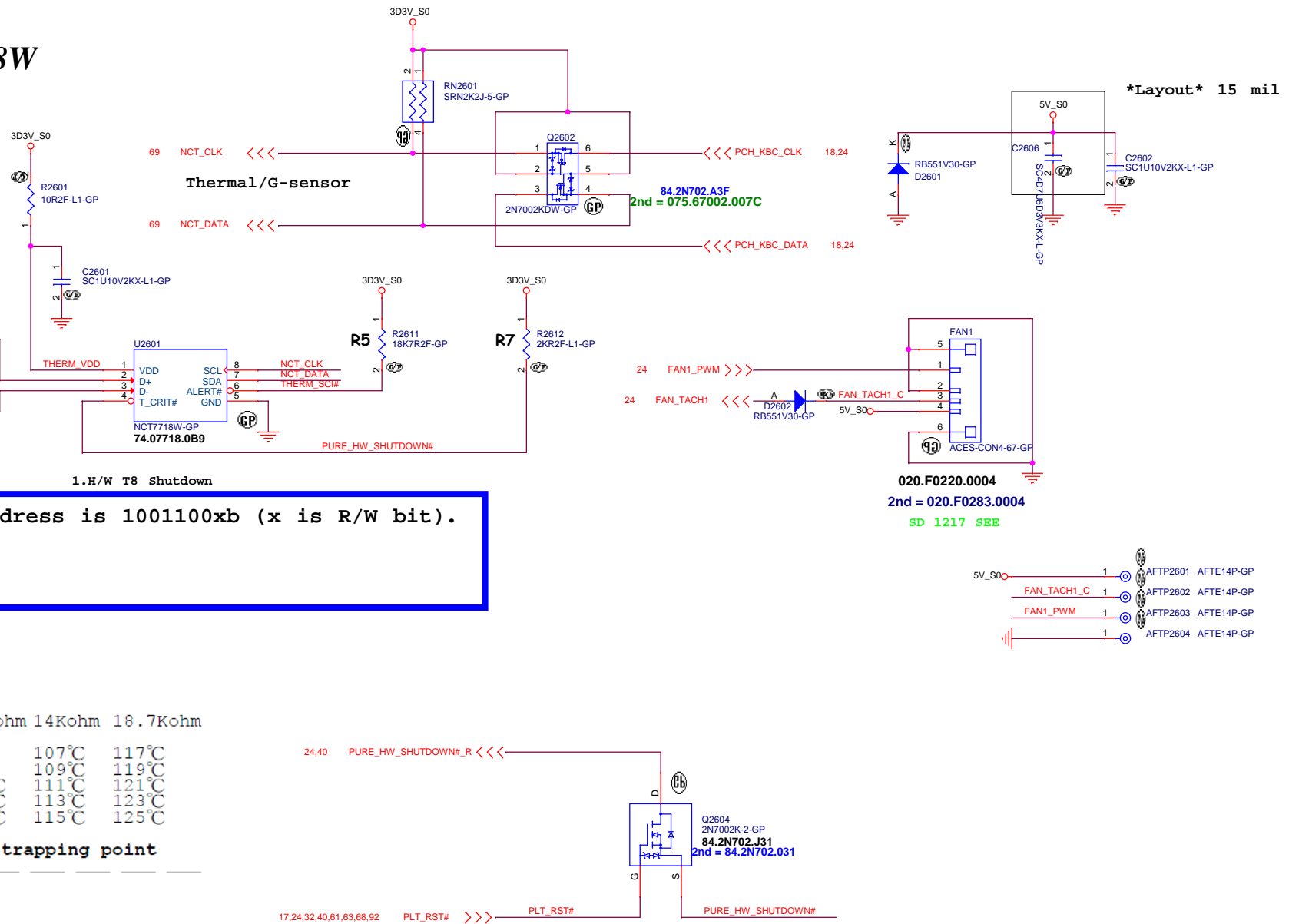
-1

Thermal sensor NCT 7718W

ALERT# /T CRIT#
Pull-up R̄esistor

	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T8=85 degree



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

G788P81/Fan Controller P2793

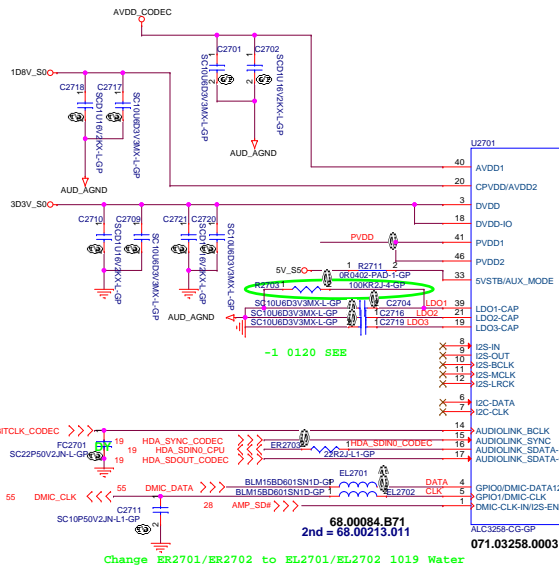
Rev

Brittle 13.3 Intel

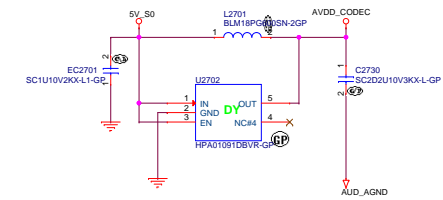
-1

Date: Thursday, February 18, 2016

Sheet 26 of 107



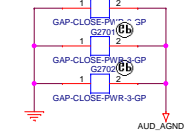
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



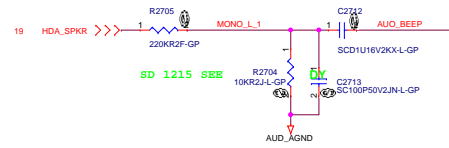
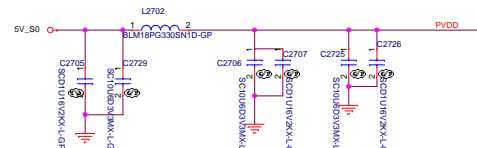
Digital GND & AUD_AGND

Tie Analog GND and Digital GND under codec by a single point

Add G2703 10/21 water

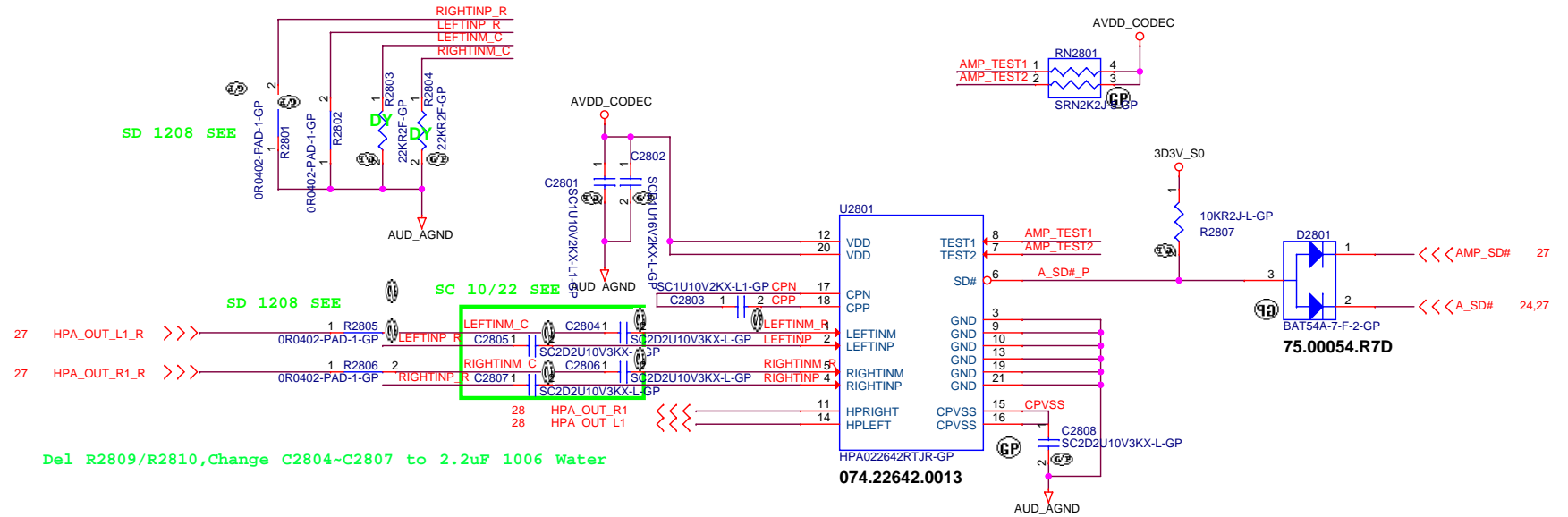


audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

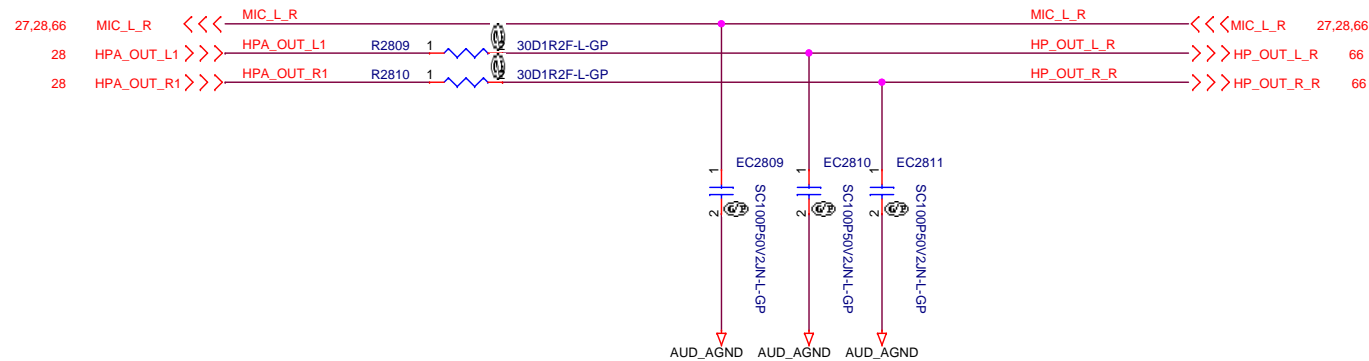


<Core Design>

AMP. for Headphone



Combo-Jack (Headphone & MIC)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

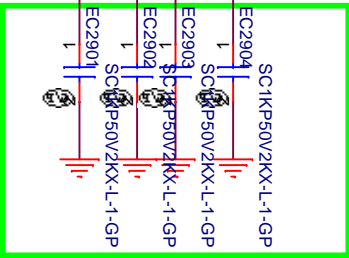
Title		
Audio AMP HPA0022642RTJR		
Size	Document Number	Rev
B		-1
Date: Thursday, February 18, 2016		
Sheet 28 of 107		

SPK Connector

SD 1215 SEE

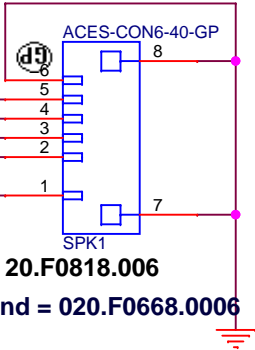
SPK Vendor	FG	Sable
SPK_ID	1	0

18,24 SPK_ID
27 SPKR_L+
27 SPKR_L-
27 SPKR_R+
27 SPKR_R-

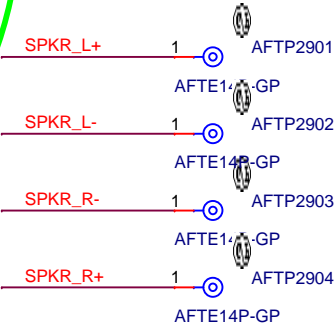


Change C2901~C2904 to EC2901~EC2904 10/21 water

Speaker



-1 0121 SEE



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio SPK Conn

Size

A4

Document Number

Brittle 13.3 Intel

Date

Thursday, February 18, 2016

Sheet

29

of

107

Rev

-1

(Blanking)

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN(NA)

Size

Document

Number

Rev

A3

Brittle 13.3 Intel

-1

Date: Thursday, February 18, 2016

Sheet 30 of 107

(Blanking)

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(LAN+VGA) NA

Size
A3

Document Number

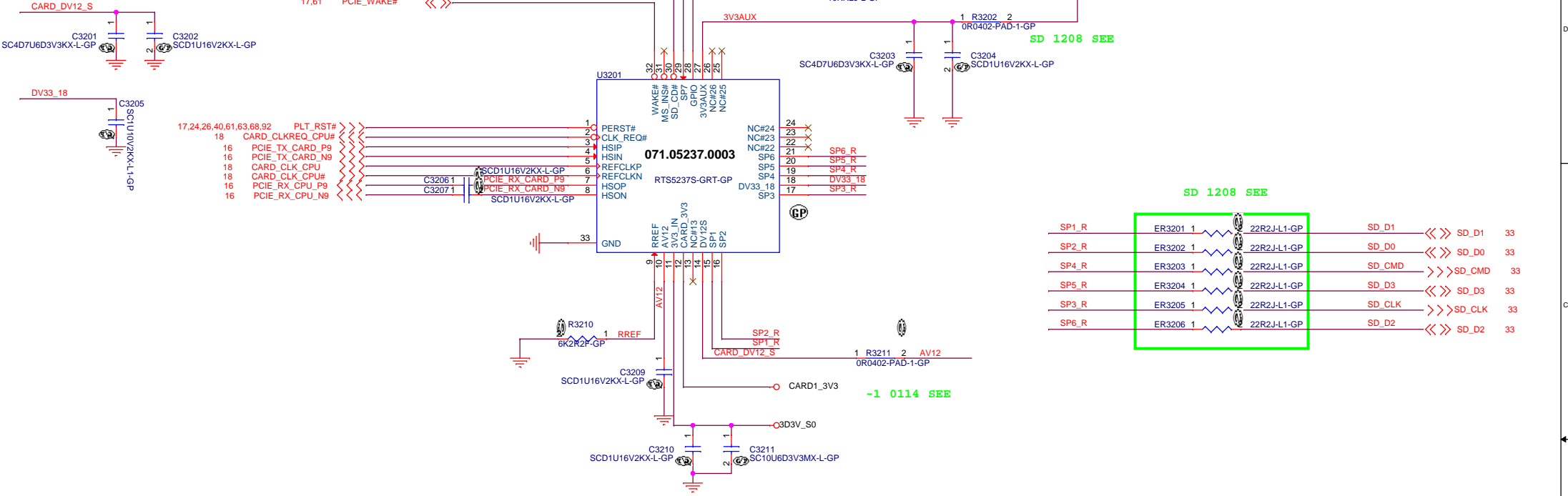
Rev
-1

Date: Thursday, February 18, 2016

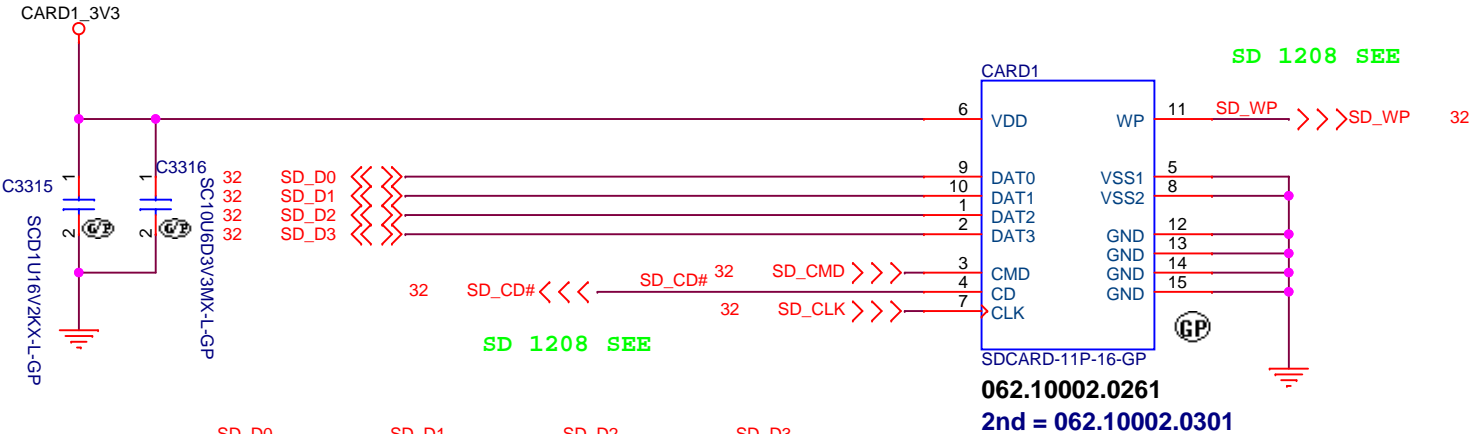
Sheet 31 of 107

Cardreader IC & Cardreader Connector

SSID = CardReader

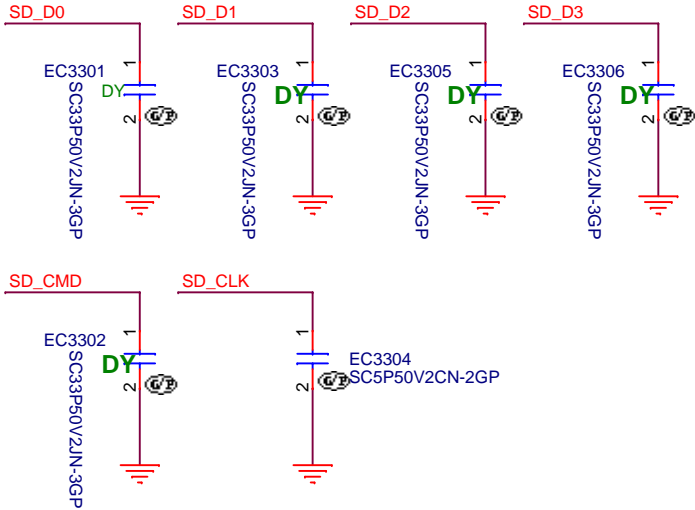


SSID = CardReader

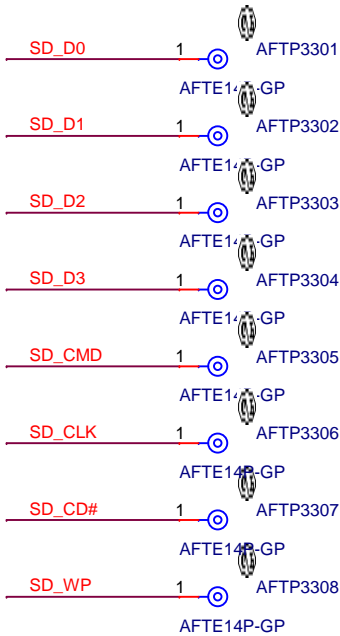


WP	Protect	Write
IC	H	L
Conn	H	L

CD#	Plug	Un-Plug
IC	L	H
Conn	L	H



Connector Pin No.	SD Card Pin No.	Pin Define
P1	P9	DAT2
P2	P1	DAT3
P3	P2	CMD
P4		CD
P5	P3	VSS1
P6	P4	VDD
P7	P5	CLK
P8	P6	VSS2
P9	P7	DAT0
P10	P8	DAT1
P11		W/P
P12		GND
P13		GND
P14		GND
P15		GND



with out card	CD	CD
	WP	WP
inserted card (unlock)	CD	CD
	WP	WP
inserted card(lock)	CD	CD
	WP	WP

SD 1208 SEE

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size A4

Document Number

Rev -1

Date: Thursday, February 18, 2016

Sheet 33 of 107

Brittle 13.3 Intel

USB 3.0

Delete Type C logic part 0817 Water

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB CHARGER IC

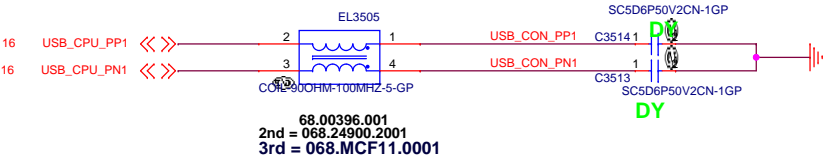
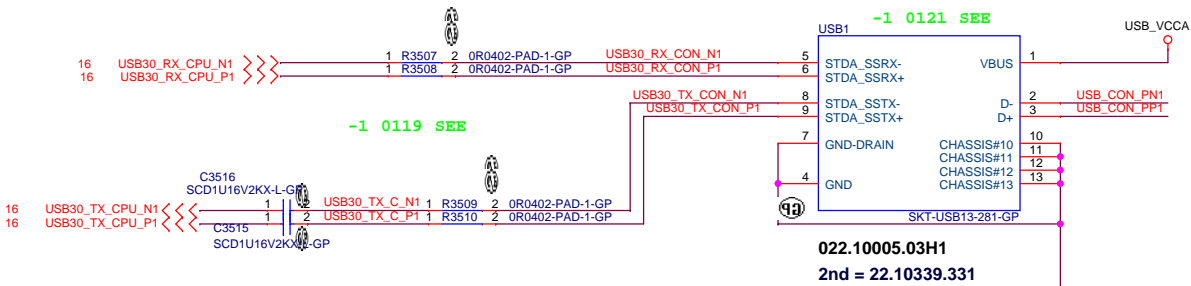
Size
A3

Document Number

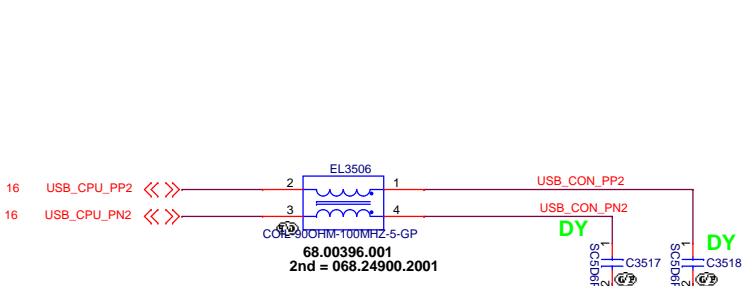
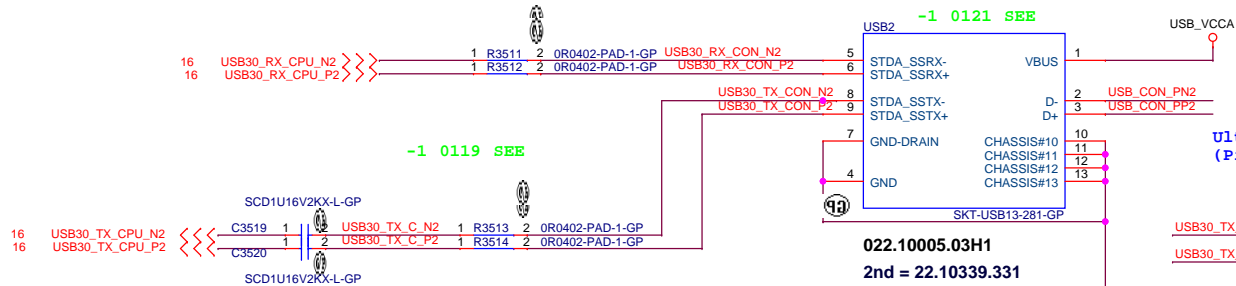
Rev
-1

Date: Thursday, February 18, 2016

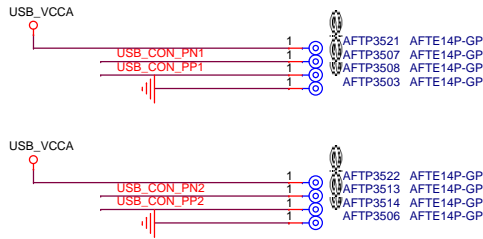
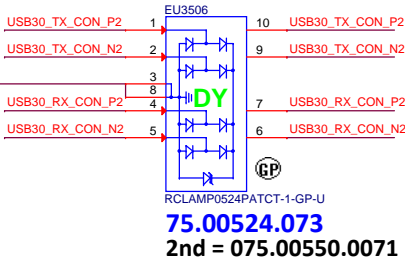
Sheet 34 of 107



Right



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



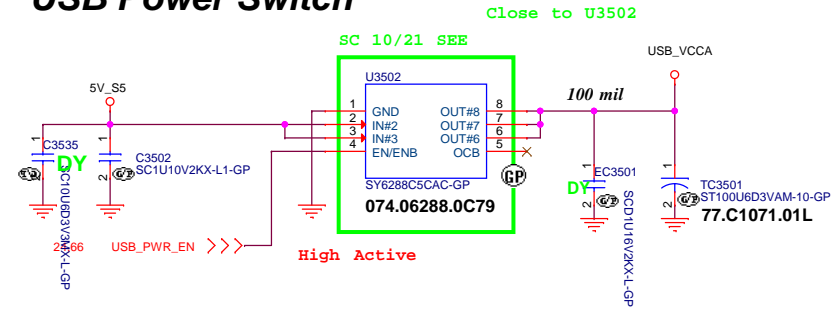
USB Table

Pair	Device
0	USB3.0 Port 1
1	USB3.0 Port 2
2	USB2.0 Port 3
3	CCD Port 4/8
4	WLAN(Bluetooth) Port 6
5	Sensor Hub Port 5

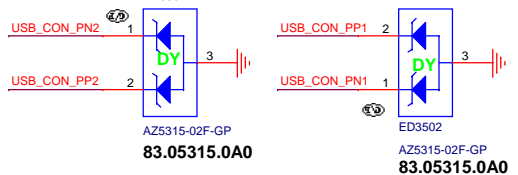
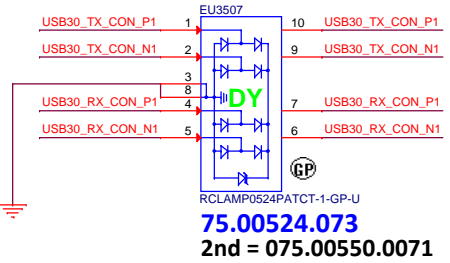
USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB Power Switch

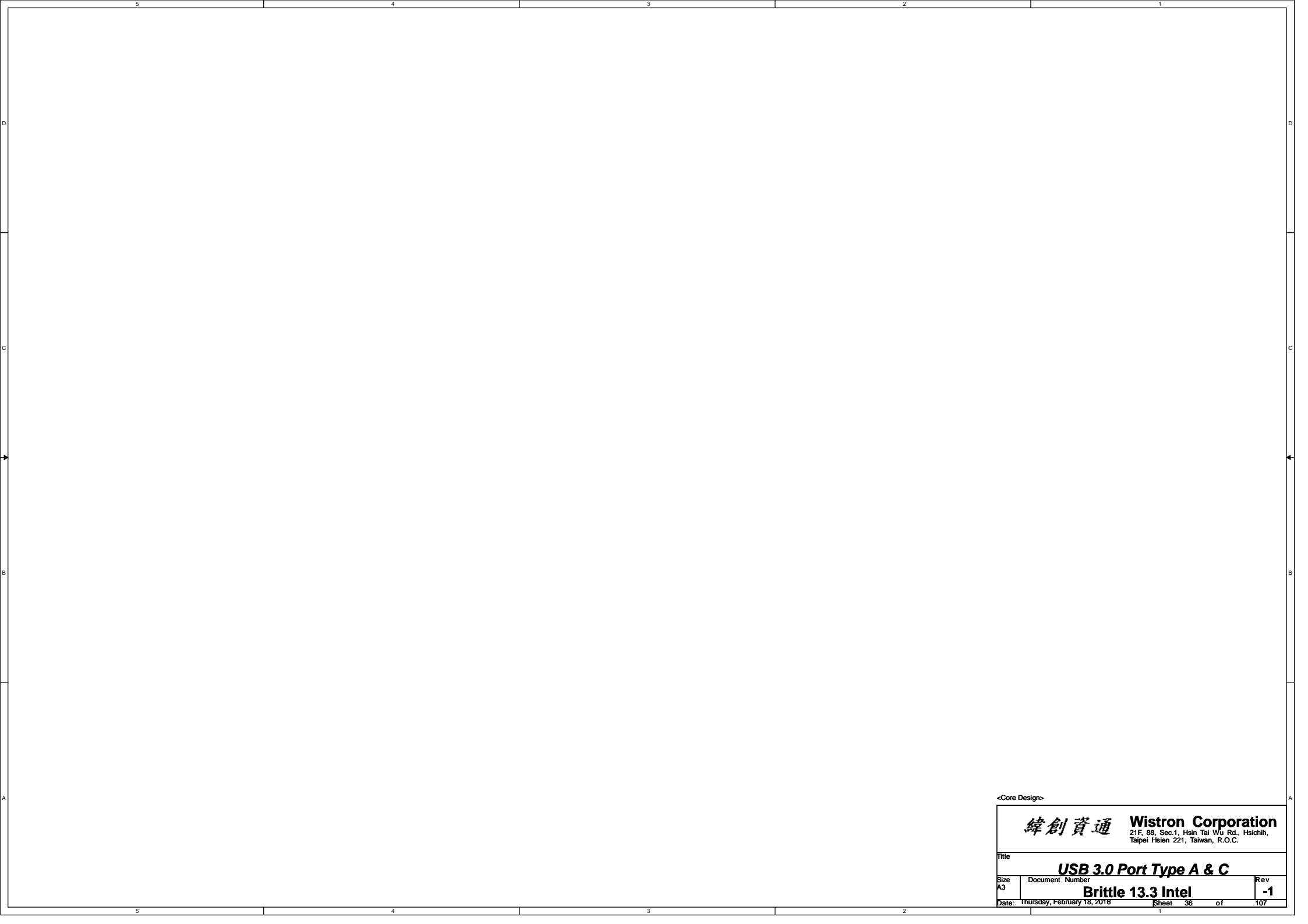


Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 3.0 Port Type A & C			
Size	Document	Number	Rev
A3	Brittle 13.3 Intel		-1
Date:	Thursday, February 18, 2016		
	Sheet	36	of 107

USB 3.0 Redriver_Intel

Delete Redriver part 0817 Water

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB 3.0 Redriver

Size
A3

Document Number

Rev
-1

Date: Thursday, February 18, 2016

Sheet 37 of 107

5	4	3	2	1
D				D
C				C
B				B
A				A

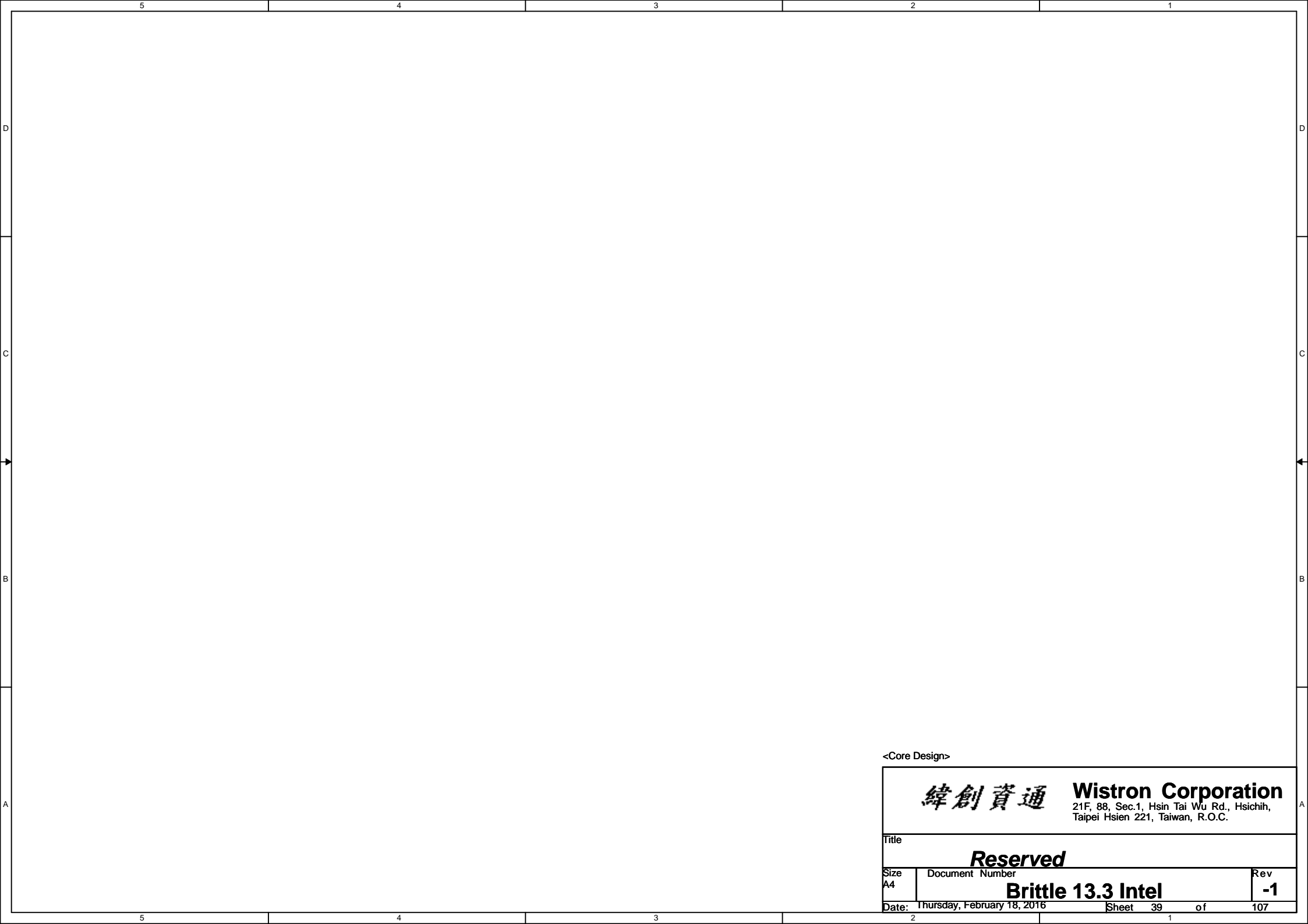
<Core Design>

Wistron Confidential document, Anyone can not
Duplicate, Modify, Forward or any other
application without get Wistron permis

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ADAPTER OCP / S3 reduction		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016	Sheet 38 of	107



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size A4	Document Number Brittle 13.3 Intel	Rev -1
------------	--	------------------

(Blanking)

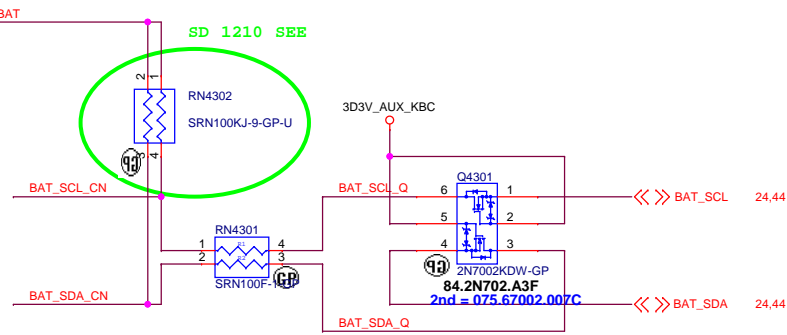
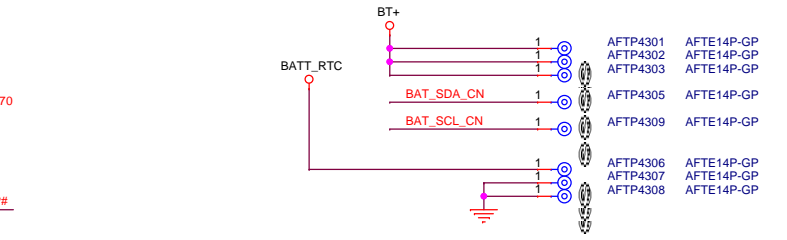
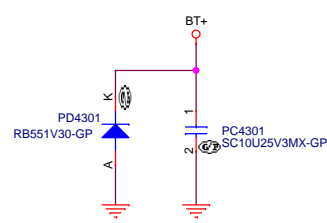
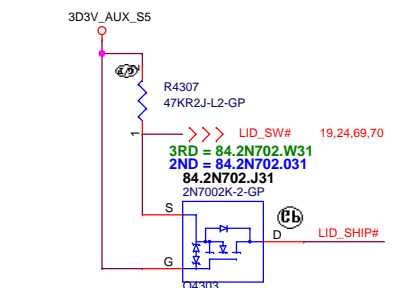
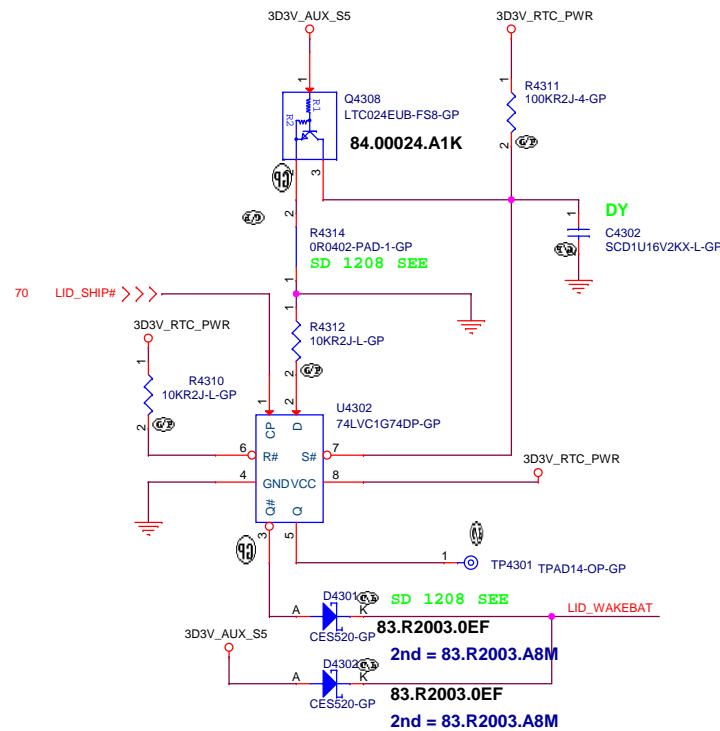
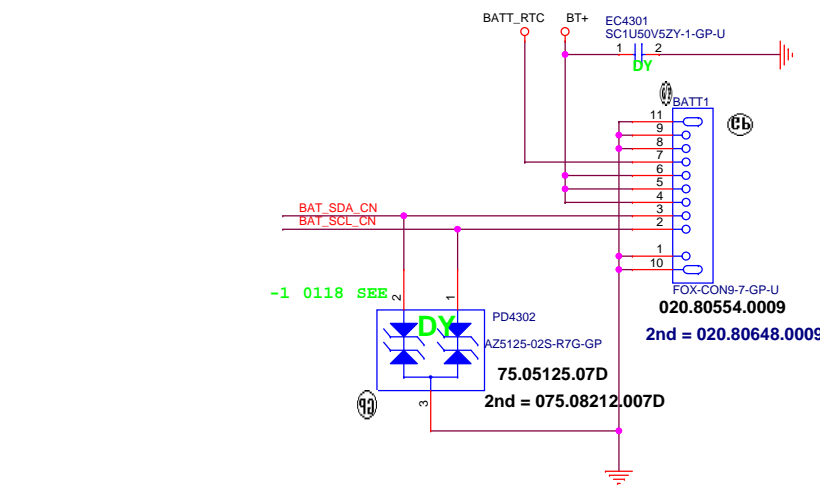
Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
DS3		
Size	Document Number	Rev
A4	Brittle 13.3 Intel	-1
Date:	Thursday, February 18, 2016	Sheet 41 of 107

Battery Connector

Check Battery Pin Spec



Pin No.	Symbol	Description
1	GND	Batt-, Battery Negative Terminal
2	B/I	Connected to GND
3	RTC	Connected to REG33 at Pin #24 of G/G IC, 3.3V supply output
456	BATT+	Batt+, Battery Positive Terminal
7	SMD	SMBus data interface I/O pin.
8	SMC	SMBus clock interface I/O pin.
9	GND	Batt-, Battery Negative Terminal

<Core Design>

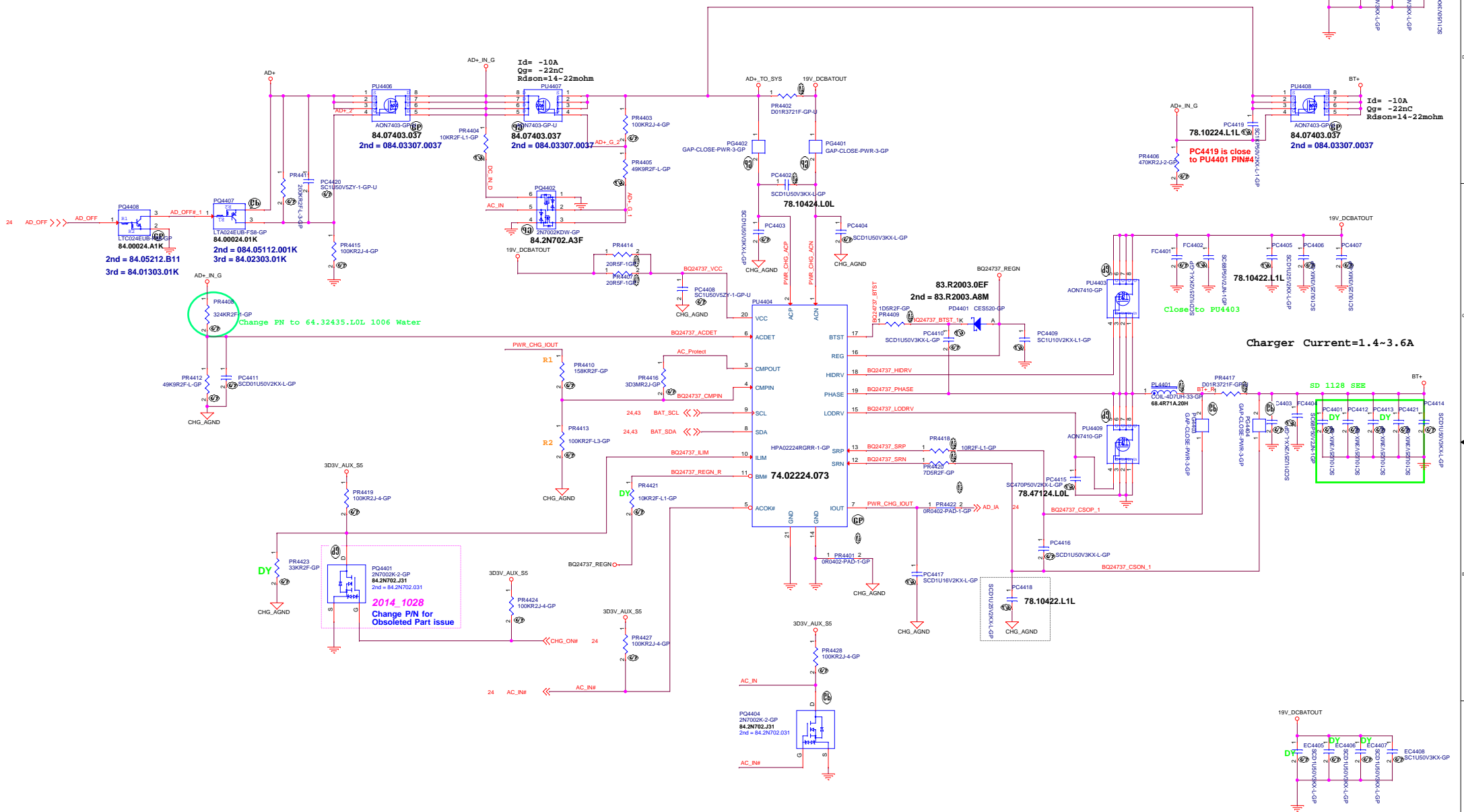
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title BATT CONN

Size A3 Document Number Rev -1

Date: Thursday, February 18, 2016 Sheet 43 of 107

SSID = Charger



&ltCore Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Charger HPA02224RGRR			
Size A2	Document Number	Rev	
	Brittle 13.3 Intel	-1	
Date:	Thursday, February 18, 2016	Sheet 44	of 107

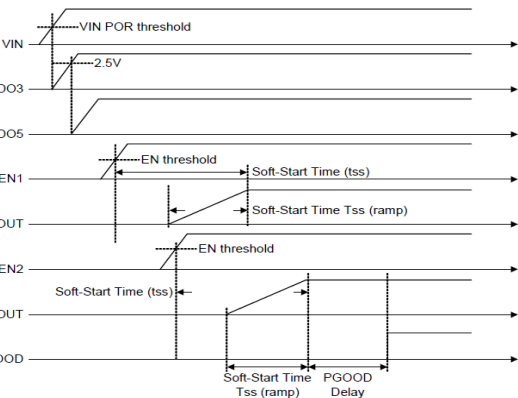
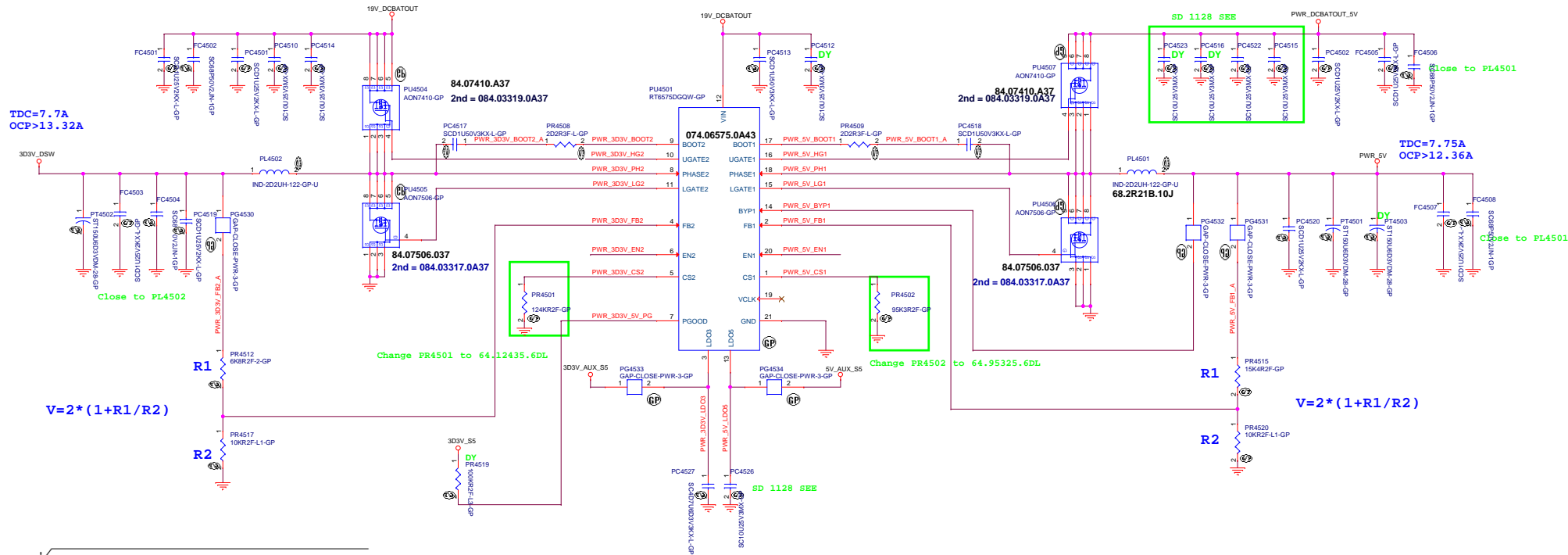
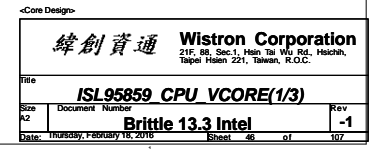
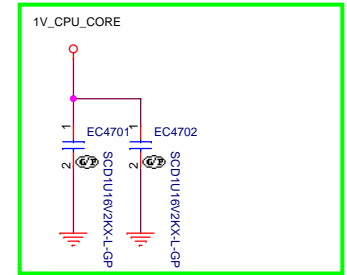
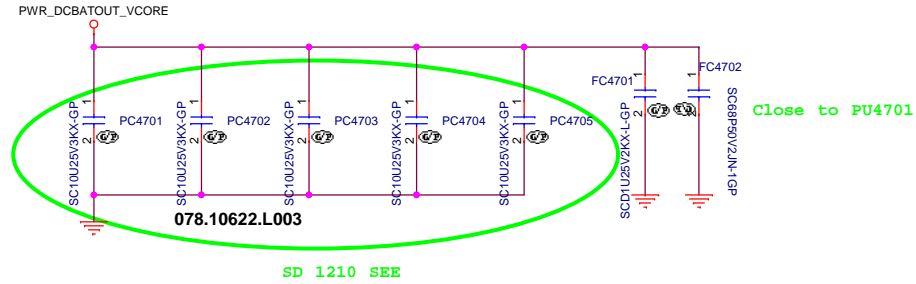
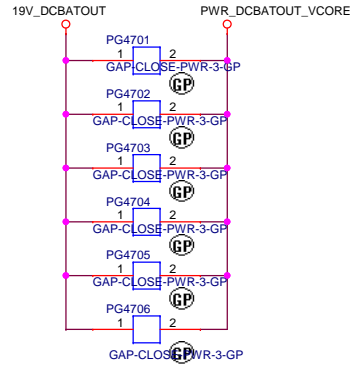


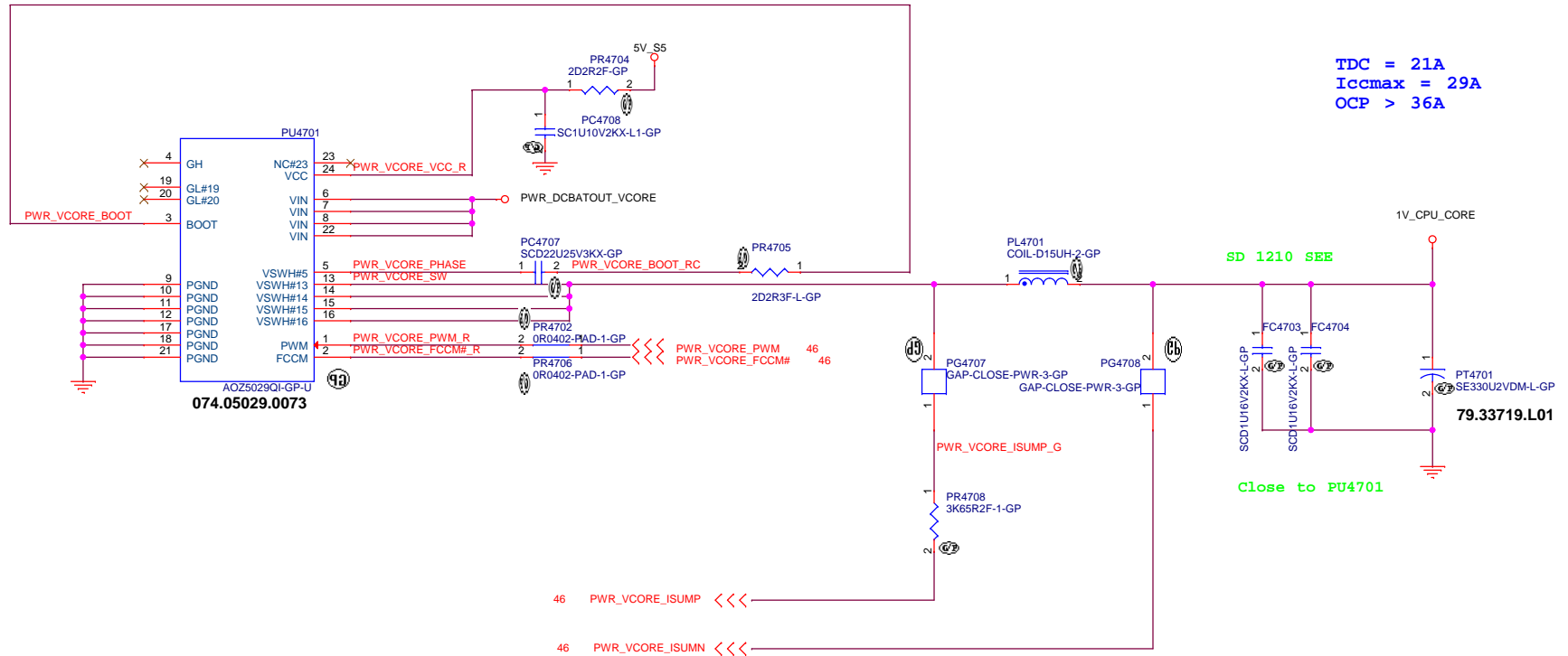
Figure 6. RT6575B Timing

[illegible]

Main Func = CPU_CORE



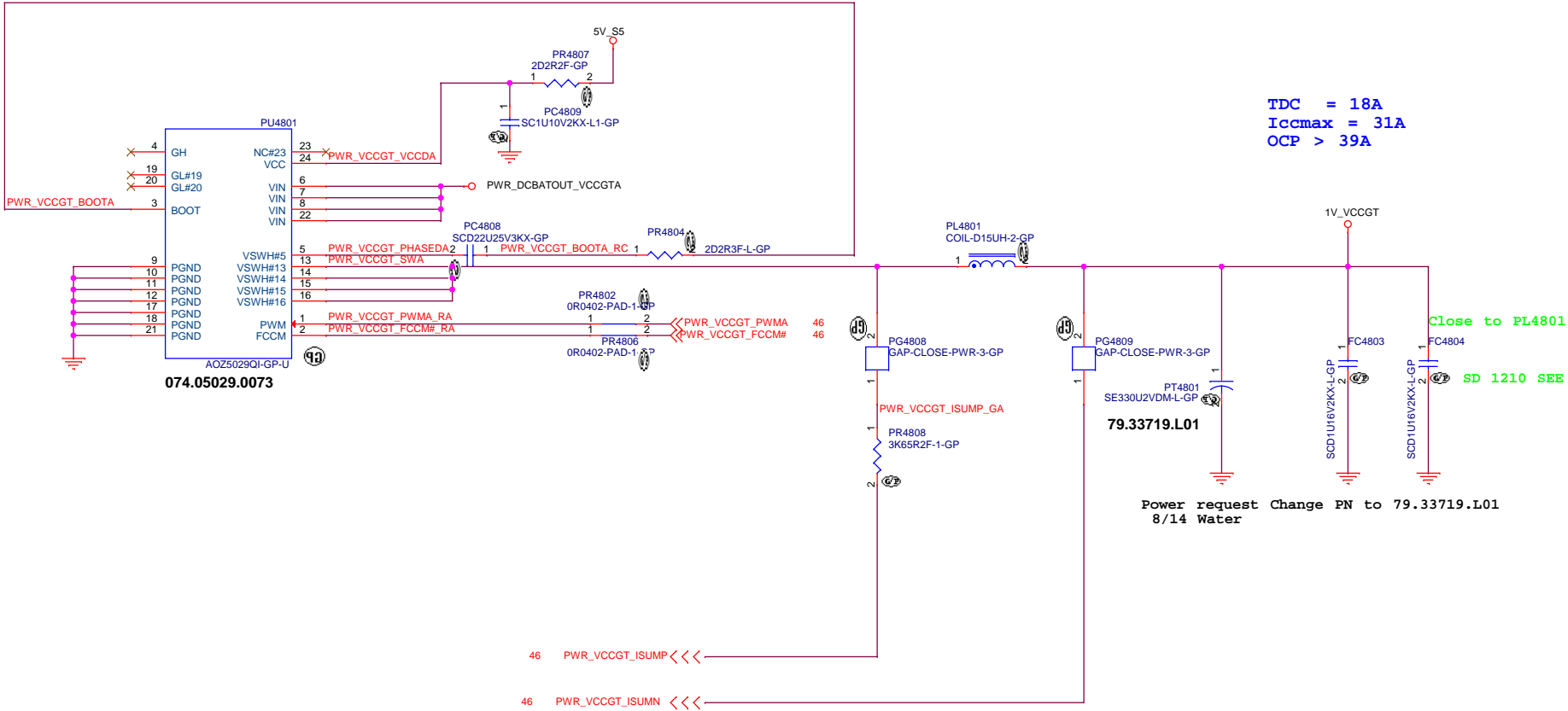
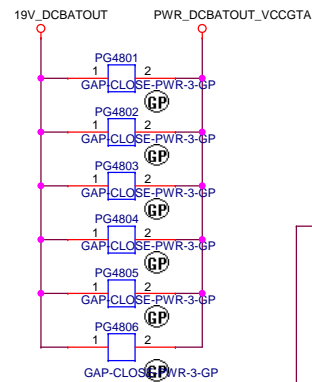
TDC = 21A
Iccmax = 29A
OCP > 36A

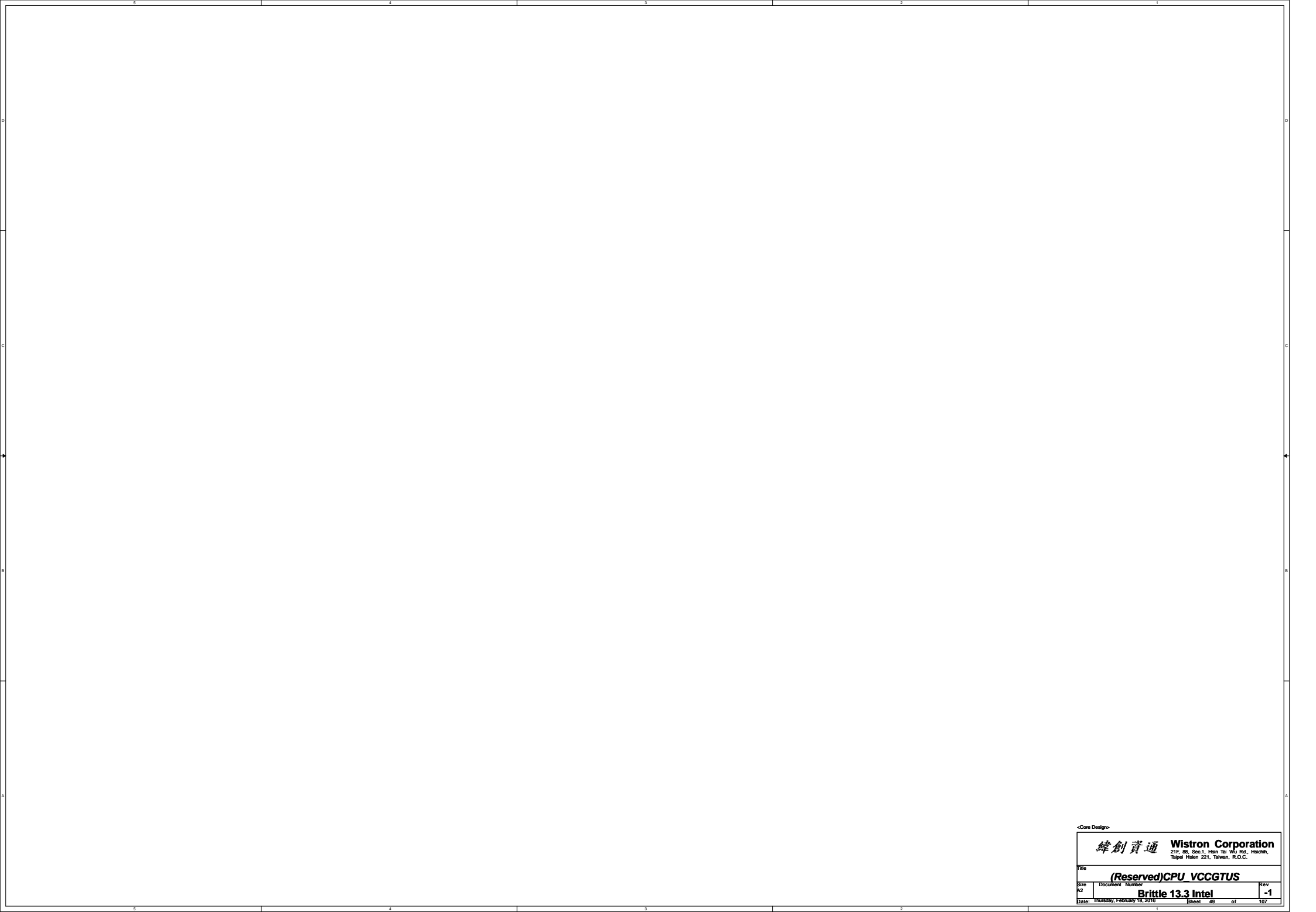


<Core Design>

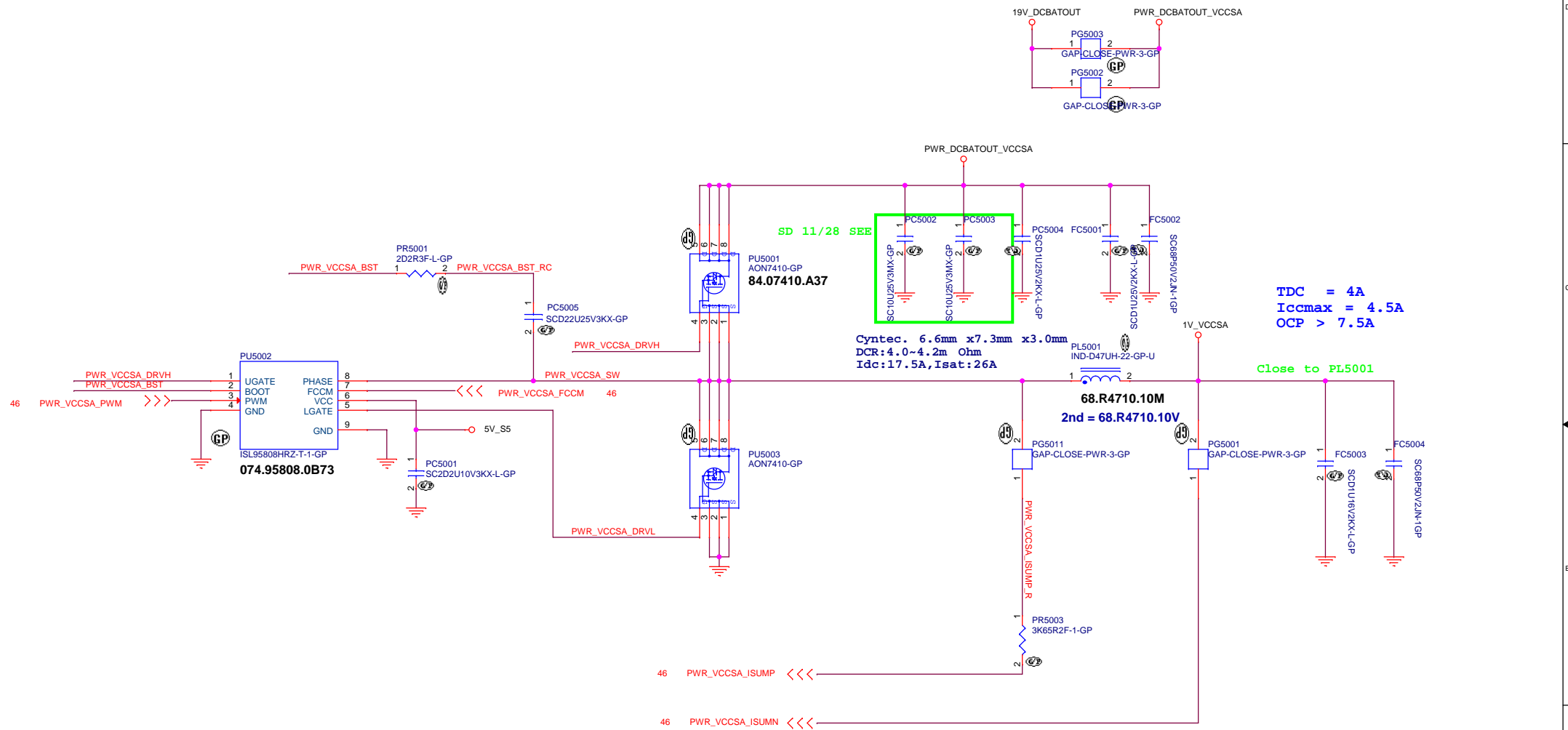
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AOZ5029QI CPU VCORE(2/3)			
Size	Document Number	Rev	
A3		-1	
Brittle 13.3 Intel			
Date:	Thursday, February 18, 2016	Sheet	47 of 107

Main Func = CPU_CORE





Main Func = CPU_CORE

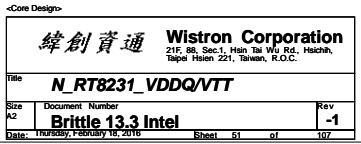


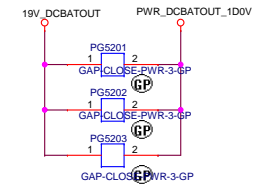
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ISL95808_CPU_VCCSA

Size A3	Document Number	Rev
Date: Thursday, February 18, 2016	Brittle 13.3 Intel	-1
Sheet 50	of 107	

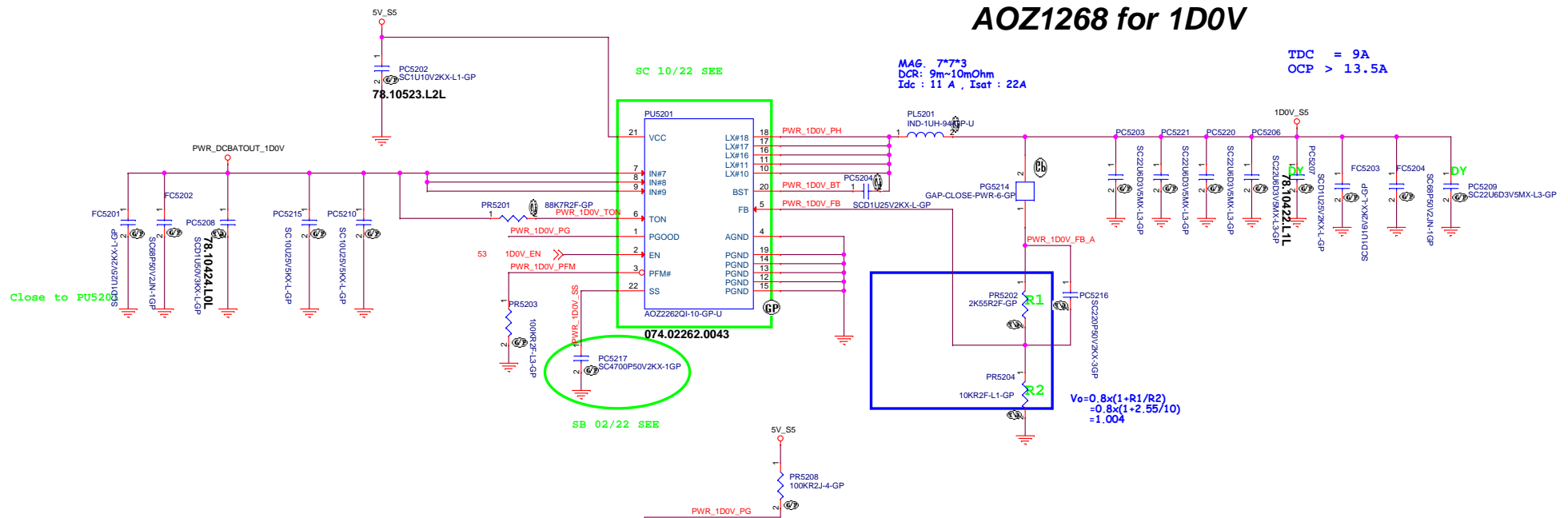




AOZ1268 for 1D0V

MAG. 7*7*3
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

TDC = 9A
OCP > 13.5A



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
AOZ1268 1D0V			
Size	Document Number		Rev
Custom	Brittle 13.3 Intel		-1
Date:	Monday, February 22, 2016	Sheet 52 of	107

1D8V_S5

SC 1027 EE

PW5309
2D2R2F-GP

PC5310
SC1U10V2KX-L1-GP

3D3V_S5

PR5310
10KR2F-L1-GP

1D0V_EN_R

R5301
200R2F-L1-GP

C5301
SCD1U16V2KX-L1-GP

1D0V_EN << <

PU5301
G9661-25ADJRE1U-GP
074.09661.0033
2nd = 074.05932.0033

VPP NC#1
VO#2 NC#9
VIN VO#3
VEN ADJ
POK POK

GND

PWR_1D8V_S5_VDD

PWR_1D8V_S5_PVDD

PM_SLP_SUS#

PWR_1D8V_S5_FB

1D0V_EN_R

17,24,40

PC5304
SC1U10V2KX-L1-GP

PC5302
SC10U6D3V3MX-L1-GP

PC5303
SC22P50V2JN-L1-GP

FC5301
SCD1U16V2KX-L1-GP

FC5302
SC68P50V2LN1-GP

Close to PU5301

R1
PR5302
12K7R2F-GP

R2
PR5301
10KR2F-L1-GP

PC5305
SC22P50V2JN-L1-GP

PC5306
SC10U6D3V3MX-L1-GP

PC5307
SC10U6D3V3MX-L1-GP

1D8V_S5

PWR_1D8V

PG5302
GAP-CLOSE-PWR-3-GP

PG5303
GAP-CLOSE-PWR-3-GP

PG5301
GAP-CLOSE-PWR-3-GP

3D3V_DSW

$$PD = (V_{in} - V_{out}) \times I_{out}$$

$$= (3.3 - 1.8) \times 0.3A = 0.45W$$

$$PD \text{ de-rating(\%)} = 0.45W / 1.33W = 33.8\%$$

Vout Setting

$$V_{out} = 0.8 * (1 + R1/R2)$$

$$= 0.8 * (1 + 12K7 / 10K)$$

$$= 1.816V$$

<Core Design>

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G9661 1D8V
Size B	Document Number
Date: Thursday, February 18, 2016	Sheet 53 of 107
Rev -1	

1D8V_S5

SC 1027 EE

PW5309
2D2R2F-GP

PC5310
SC1U10V2KX-L1-GP

3D3V_S5

PR5310
10KR2F-L1-GP

1D0V_EN_R

R5301
200R2F-L1-GP

C5301
SCD1U16V2KX-L1-GP

1D0V_EN_L

3D3V_DSW

PG5301
GAP-CLOSE-PWR-3-GP

PC5304
SC1U10V2KX-L1-GP

PC5302
SC10U6D3V3MX-L1-GP

PC5303
SC22P50V2JN-L1-GP

17,24,40

PW5301
G9661-25ADJRE1U-GP

VPP NC#1
VO#2 NC#9
VIN VO#3
VEN ADJ
POK POK

GND

G9661-25ADJRE1U-GP

074.09661.0033

2nd = 074.05932.0033

PM_SLP_SUS#

PWR_1D8V_S5_VDD

PWR_1D8V_S5_FB

1D0V_EN_R

R1
PR5302
12K7R2F-GP

PC5305
SC22P50V2JN-L1-GP

R2
PR5301
10KR2F-L1-GP

FC5301
SCD1U16V2KX-L1-GP

FC5302
SC68P50V2LN-1GP

Close to PW5301

PD = (Vin - Vout) × Iout
= (3.3 - 1.8) × 0.3A = 0.45W
PD de-rating(%) = 0.45W / 1.33W = 33.8%

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

<Core Design>

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G9661 1D8V
Size B	Document Number
Date: Thursday, February 18, 2016	Sheet 53 of 107

[illegible][illegible][illegible][illegible][illegible][illegible]

1D8V_S5

SC 1027 EE

PW5309
2D2R2F-GP

PC5310
SC1U10V2KX-L1-GP

3D3V_S5

PR5310
10KR2F-L1-GP

R5301
200R2F-L1-GP

C5301
SCD1U16V2KX-L1-GP

1D0V_EN_R

1D0V_EN_L

3D3V_DSW

PG5301
GAP-CLOSE-PWR-3-GP

PC5304
SC1U10V2KX-L1-GP

PC5302
SC10U6D3V3MX-L1-GP

PC5303
SC22P50V2JN-L1-GP

17,24,40

PW5301
G9661-25ADJRE1U-GP

VPP NC#1
VO#2 NC#9
VIN VO#3
VEN ADJ
POK

GND

074.09661.0033
2nd = 074.05932.0033

PM_SLP_SUS#

PWR_1D8V_S5_VDD

PWR_1D8V_S5_FB

1D0V_EN_R

R1
PR5302
12K7R2F-GP

R2
PR5301
10KR2F-L1-GP

PC5305
SC22P50V2JN-L1-GP

FC5301
SCD1U16V2KX-L1-GP

FC5302
SC68P50V2LN1-GP

Close to PU5301

PD = (Vin - Vout) × Iout
= (3.3 - 1.8) × 0.3A = 0.45W
PD de-rating(%) = 0.45W / 1.33W = 33.8%

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

<Core Design>

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G9661 1D8V
Size B	Document Number
Date: Thursday, February 18, 2016	Sheet 53 of 107

[illegible][illegible][illegible][illegible][illegible]

1D8V_S5

SC 1027 EE

PW5309
2D2R2F-GP

PC5310
SC1U10V2KX-L1-GP

3D3V_S5

PR5310
10KR2F-L1-GP

1D0V_EN_R

R5301
200R2F-L1-GP

C5301
SCD1U16V2KX-L1-GP

1D0V_EN_L

3D3V_DSW

PG5301
GAP-CLOSE-PWR-3-GP

PC5304
SC1U10V2KX-L1-GP

PC5302
SC10U6D3V3MX-L1-GP

PC5303
SC22P50V2JN-L1-GP

17,24,40

PW5301
G9661-25ADJRE1U-GP

VPP NC#1
VO#2 NC#9
VIN VO#3
VEN ADJ
POK

GND

074.09661.0033
2nd = 074.05932.0033

PM_SLP_SUS#

PWR_1D8V_S5_VDD

PWR_1D8V_S5_FB

1D0V_EN_R

R1
PR5302
12K7R2F-GP

R2
PR5301
10KR2F-L1-GP

PC5305
SC22P50V2JN-L1-GP

FC5301
SCD1U16V2KX-L1-GP

FC5302
SC68P50V2LN1-GP

Close to PU5301

PD = (Vin - Vout) × Iout
= (3.3 - 1.8) × 0.3A = 0.45W
PD de-rating(%) = 0.45W / 1.33W = 33.8%

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

<Core Design>

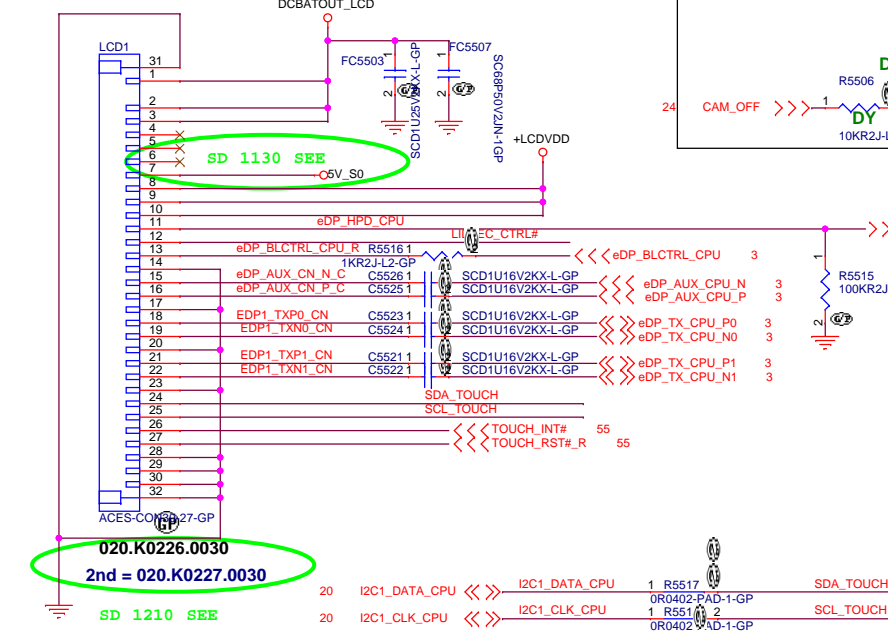
緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G9661 1D8V
Size B	Document Number
Date: Thursday, February 18, 2016	Sheet 53 of 107

SSID = 1D5V_S0

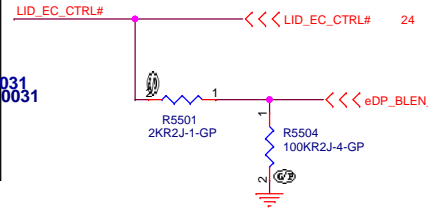
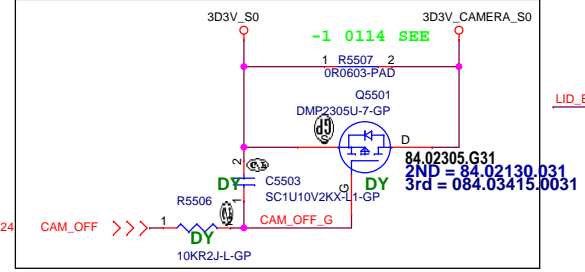
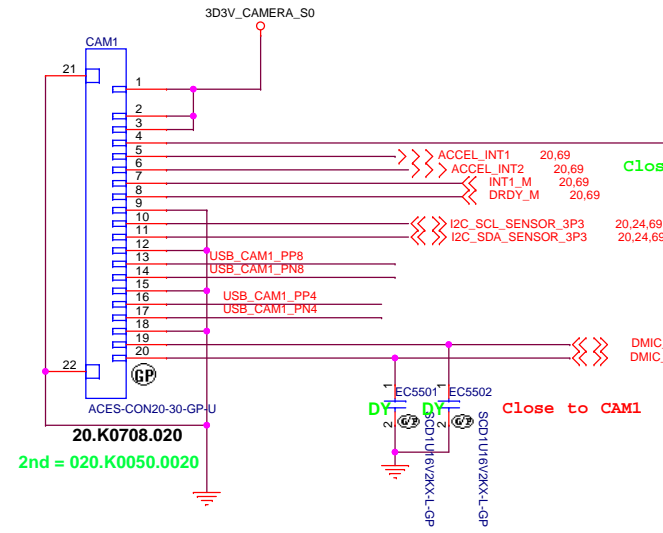
<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title 1D5V_S0		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016		Sheet 54 of 107

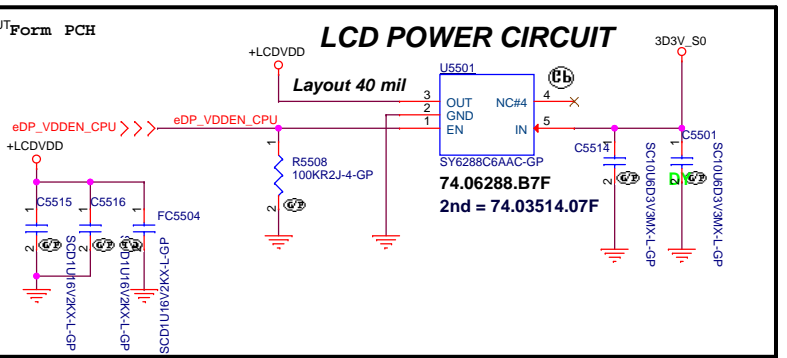
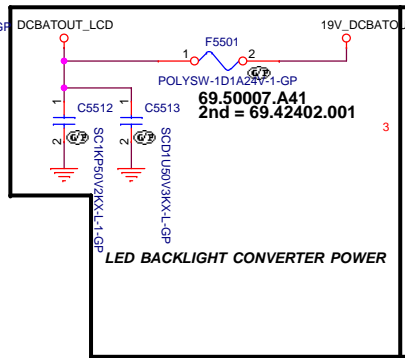
eDP+ Touch Conn



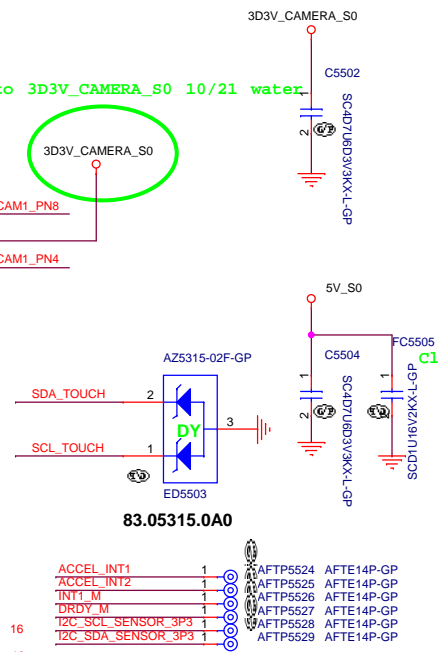
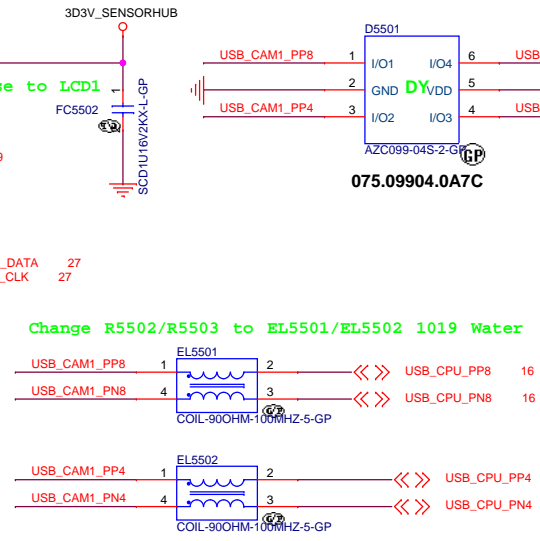
USB Camera with DMIC
I2C G-Sensor



3D3V_CAMERA_S0	1	AFTP5530	AFTE14P-GP
3D3V_S0	1	AFTP5501	AFTE14P-GP
+LCDVDD	1	AFTP5502	AFTE14P-GP
DCBATOUT_LCD	1	AFTP5522	AFTE14P-GP
	1	AFTP5503	AFTE14P-GP
USB_CAM1_PP8	1	AFTP5504	AFTE14P-GP
USB_CAM1_PN8	1	AFTP5505	AFTE14P-GP
USB_CAM1_PP4	1	AFTP5506	AFTE14P-GP
USB_CAM1_PN4	1	AFTP5507	AFTE14P-GP
SDA_TOUCH	1	AFTP5508	AFTE14P-GP
SCL_TOUCH	1	AFTP5509	AFTE14P-GP
TOUCH_INT#	1	AFTP5519	AFTE14P-GP
TOUCH_RST#_R	1	AFTP5520	AFTE14P-GP
DMIC_DATA	1	AFTP5521	AFTE14P-GP
DMIC_CLK	1	AFTP5523	AFTE14P-GP
EDP1_TXP1_CN	1	AFTP5510	AFTE14P-GP
EDP1_TXN1_CN	1	AFTP5511	AFTE14P-GP
EDP1_TXP0_CN	1	AFTP5512	AFTE14P-GP
EDP1_TXN0_CN	1	AFTP5513	AFTE14P-GP
EDP_AUX_CN_N_C	1	AFTP5514	AFTE14P-GP
EDP_AUX_CN_P_C	1	AFTP5515	AFTE14P-GP
EDP_HPDC_CPU	1	AFTP5516	AFTE14P-GP
LID_EC_CTRL#	1	AFTP5517	AFTE14P-GP
EDP_BLCtrl_CPU_R	1	AFTP5518	AFTE14P-GP



Change power Plane to 3D3V_CAMERA_S0 10/21 water



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EDP Connector + Webcam**

Size: A3 Document Number: **Brittle 13.3 Intel** Rev: -1

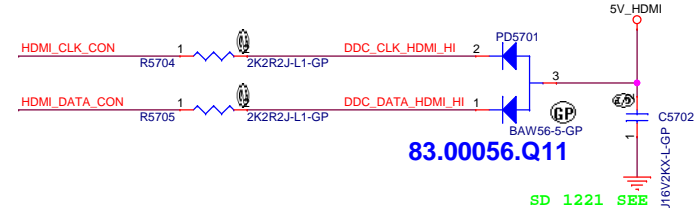
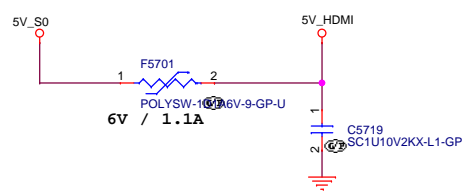
Date: Thursday, February 18, 2016 Sheet: 55 of 107

(Blanking)

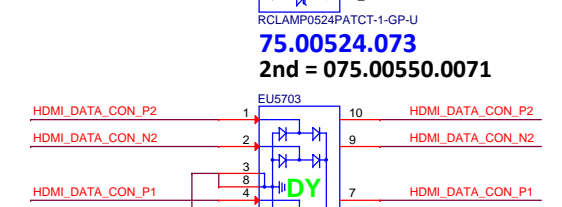
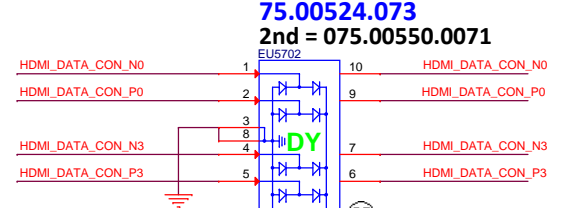
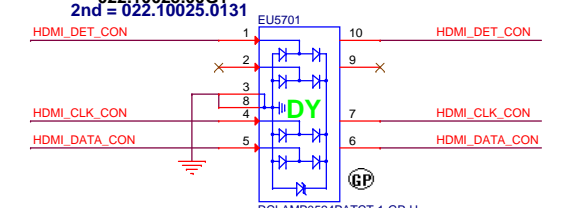
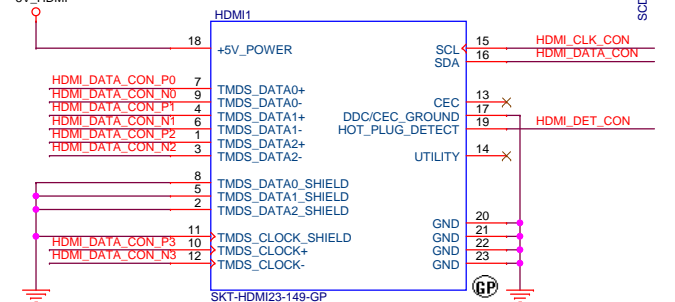
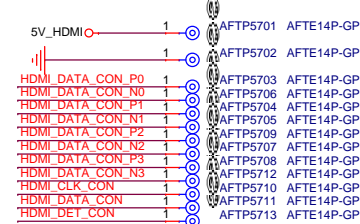
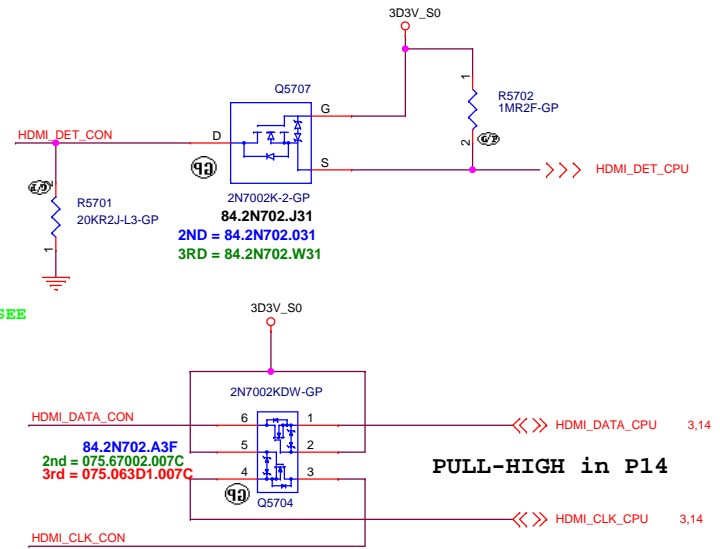
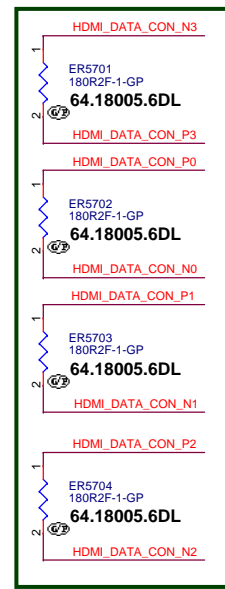
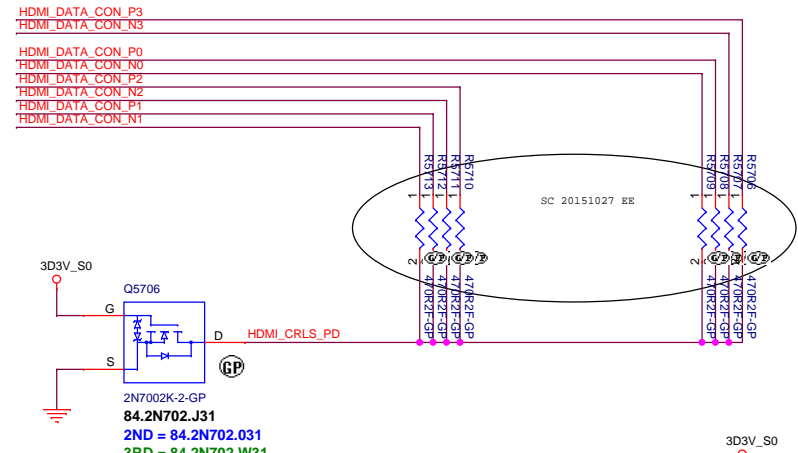
<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>(Reserved)CRT Board CN</div>		
Size <div>A4</div>	Document Number <div>Brittle 13.3 Intel</div>	Rev <div>-1</div>
Date: Thursday, February 18, 2016		Sheet 56 of 107

HDMI PS8201



3	HDMI_DATA_CPU_P0	>>>	C5711	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_P0
3	HDMI_DATA_CPU_N0	>>>	C5712	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_N0
3	HDMI_DATA_CPU_P1	>>>	C5713	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_P1
3	HDMI_DATA_CPU_N1	>>>	C5714	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_N1
3	HDMI_DATA_CPU_P2	>>>	C5715	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_P2
3	HDMI_DATA_CPU_N2	>>>	C5716	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_N2
3	HDMI_DATA_CPU_P3	>>>	C5717	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_P3
3	HDMI_DATA_CPU_N3	>>>	C5718	1	SCD1U16V2KX-L-GP	HDMI_DATA_CON_N3



<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A3 Document Number: Brittle 13.3 Intel Rev: -1

Date: Thursday, February 18, 2016 Sheet: 57 of 107

(Blanking)

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

EDP to LVDS(NA)

Size Custom

Document Number

Rev

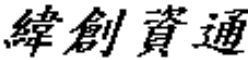
Date: Thursday, February 18, 2016

Sheet 58 of 107

-1

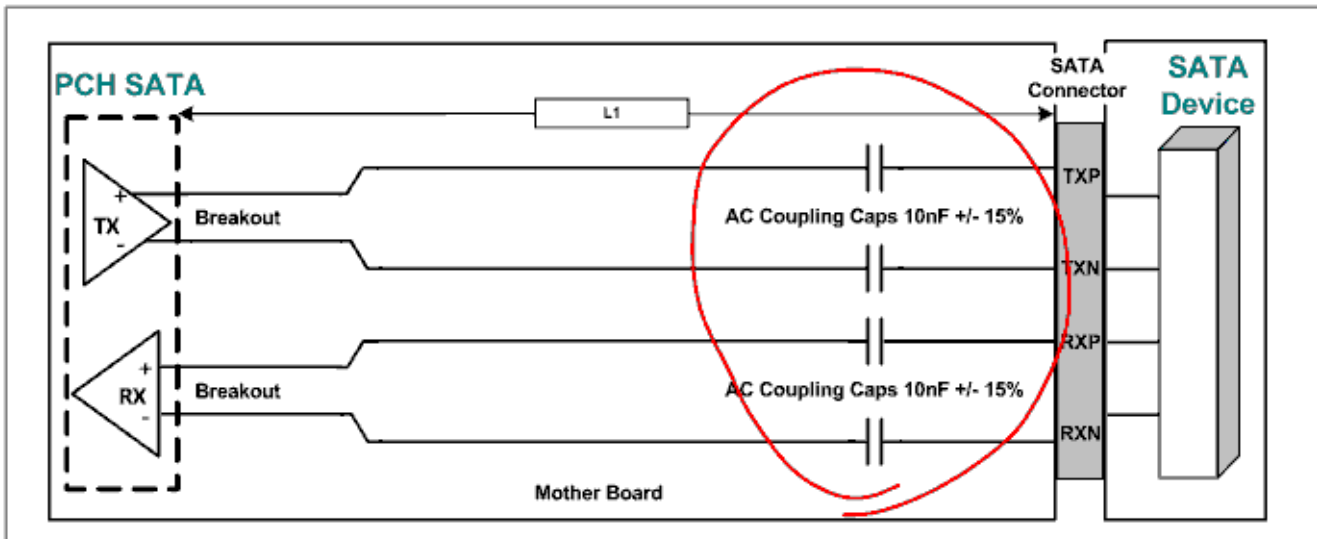
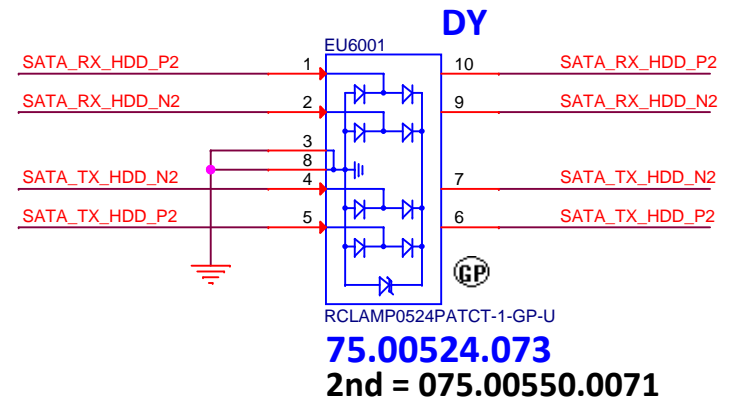
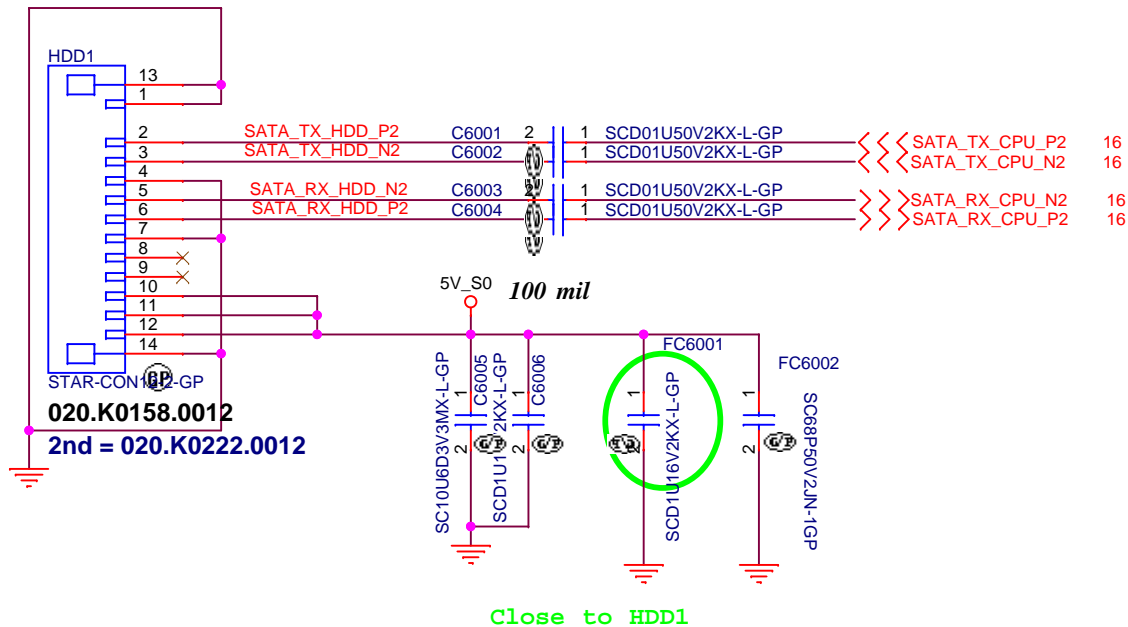
(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
DVI		
Size A	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016	Sheet 59 of	107

SSID = SATA

SATA HDD Connector



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SATA HDD

Size
A4

Document Number

Brittle 13.3 Intel

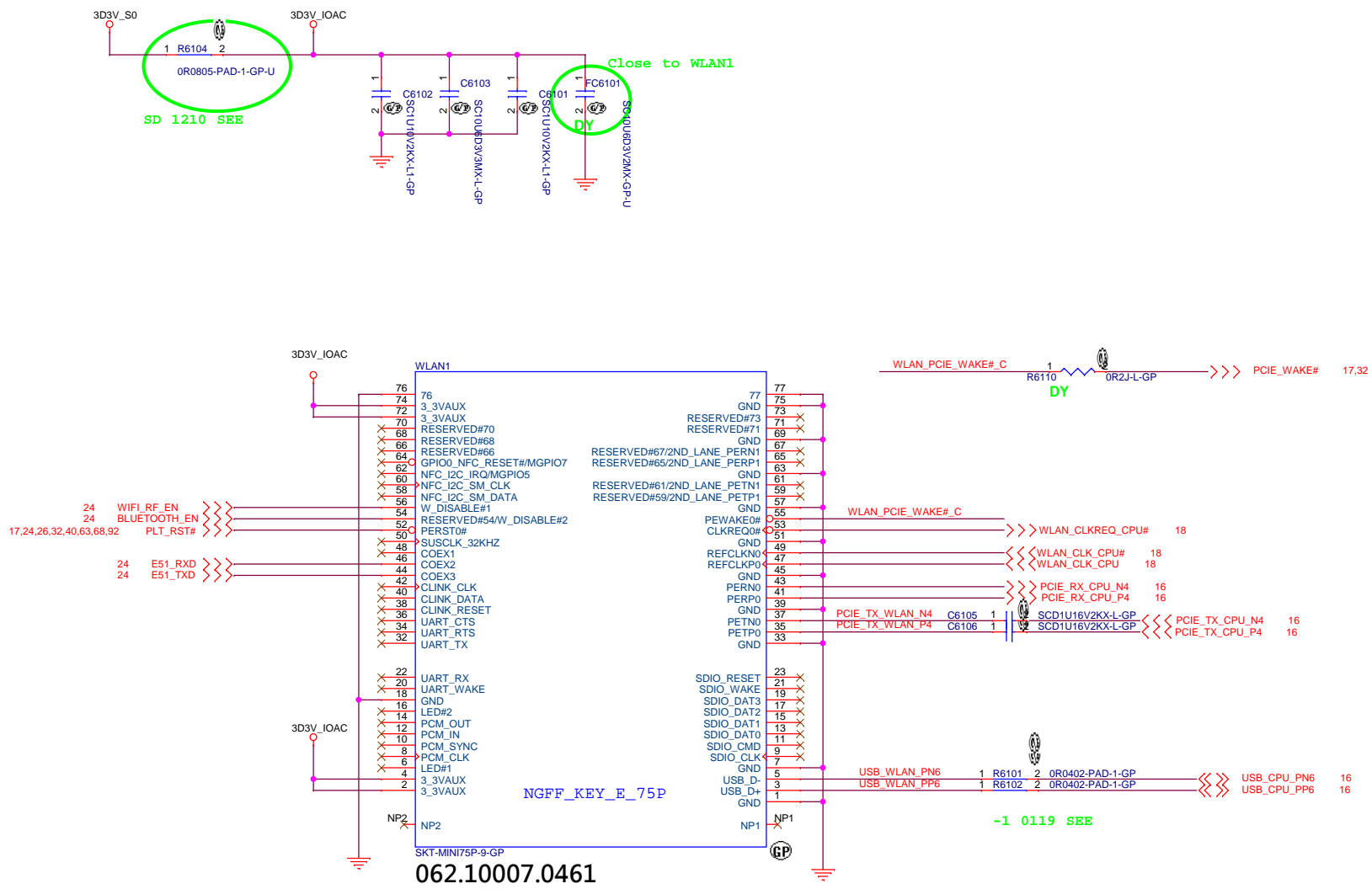
Rev
-1

Date: Thursday, February 18, 2016

Sheet 60 of 107

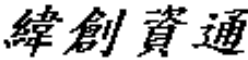
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



(Blanking)

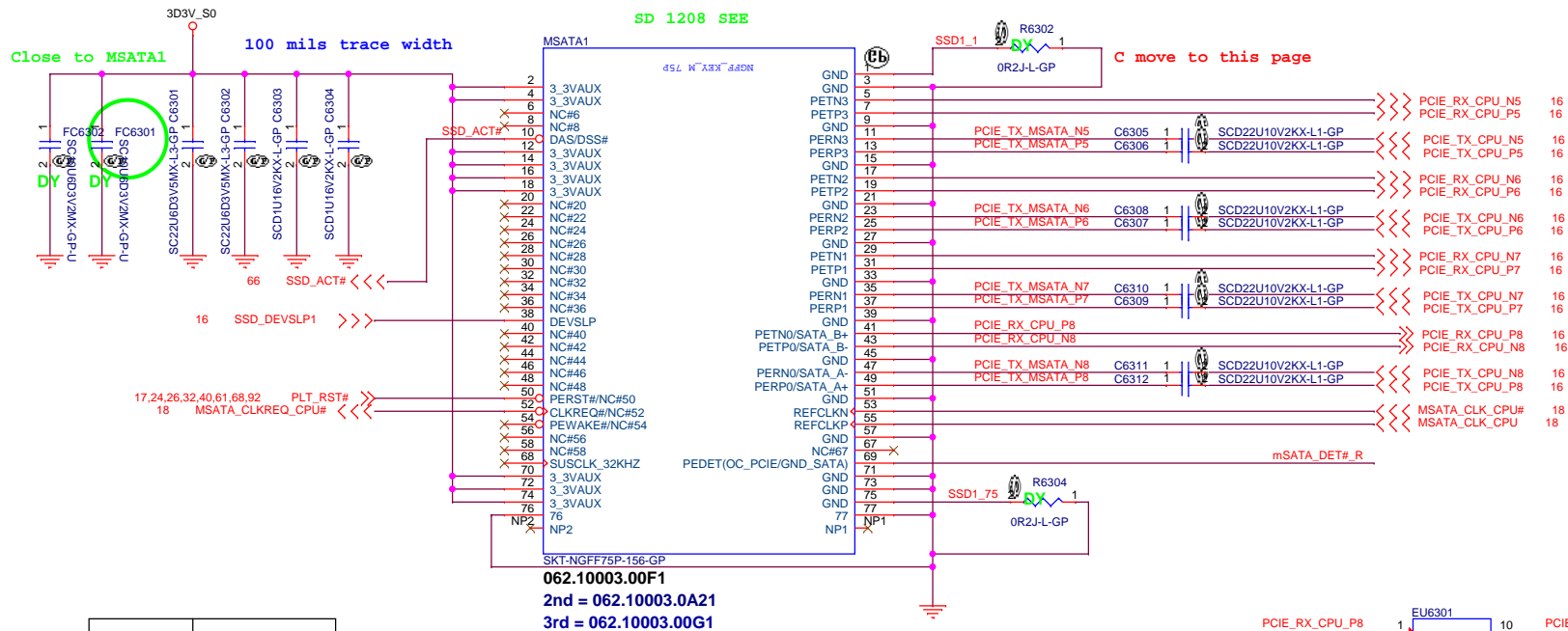
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Wireless Charging			
Size A	Document Number Brittle 13.3 Intel		Rev -1
Date: Thursday, February 18, 2016		Sheet 62 of	107

NGFF Connector

SSD slot C key M 2280-S3

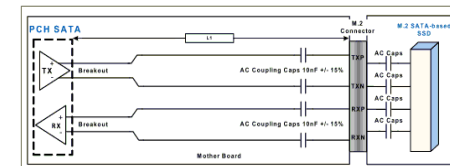
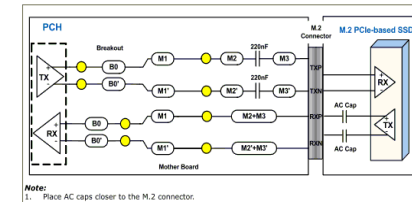
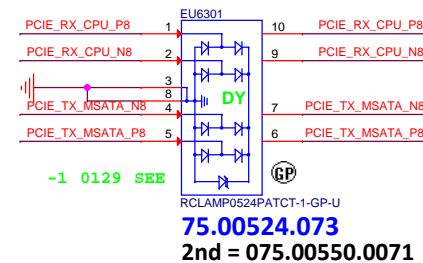
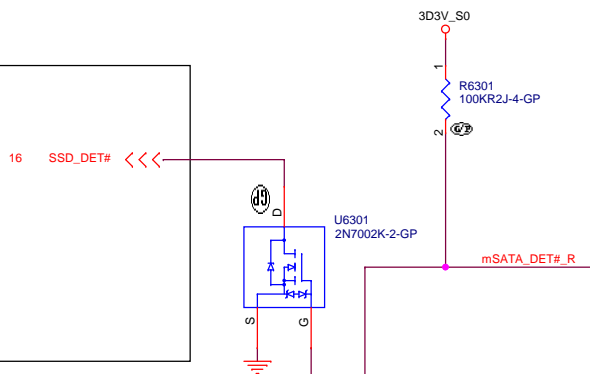
20150713 Add Truth Table and modify direction



power supply	3.3V
Active Power	50mA / 0.165W SAMSUNG 45mA/0.15mW Intel
Idle Power	43mA / 142mW SAMSUNG 22mA/75mW Intel

mSATA_DET	
1	SATA
0	PCIe

20150713 Add Truth Table and modify direction



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

mSATA Connector

Size
A3

Document Number

Brittle 13.3 Intel

Date: Thursday, February 18, 2016

Sheet 63 of 107

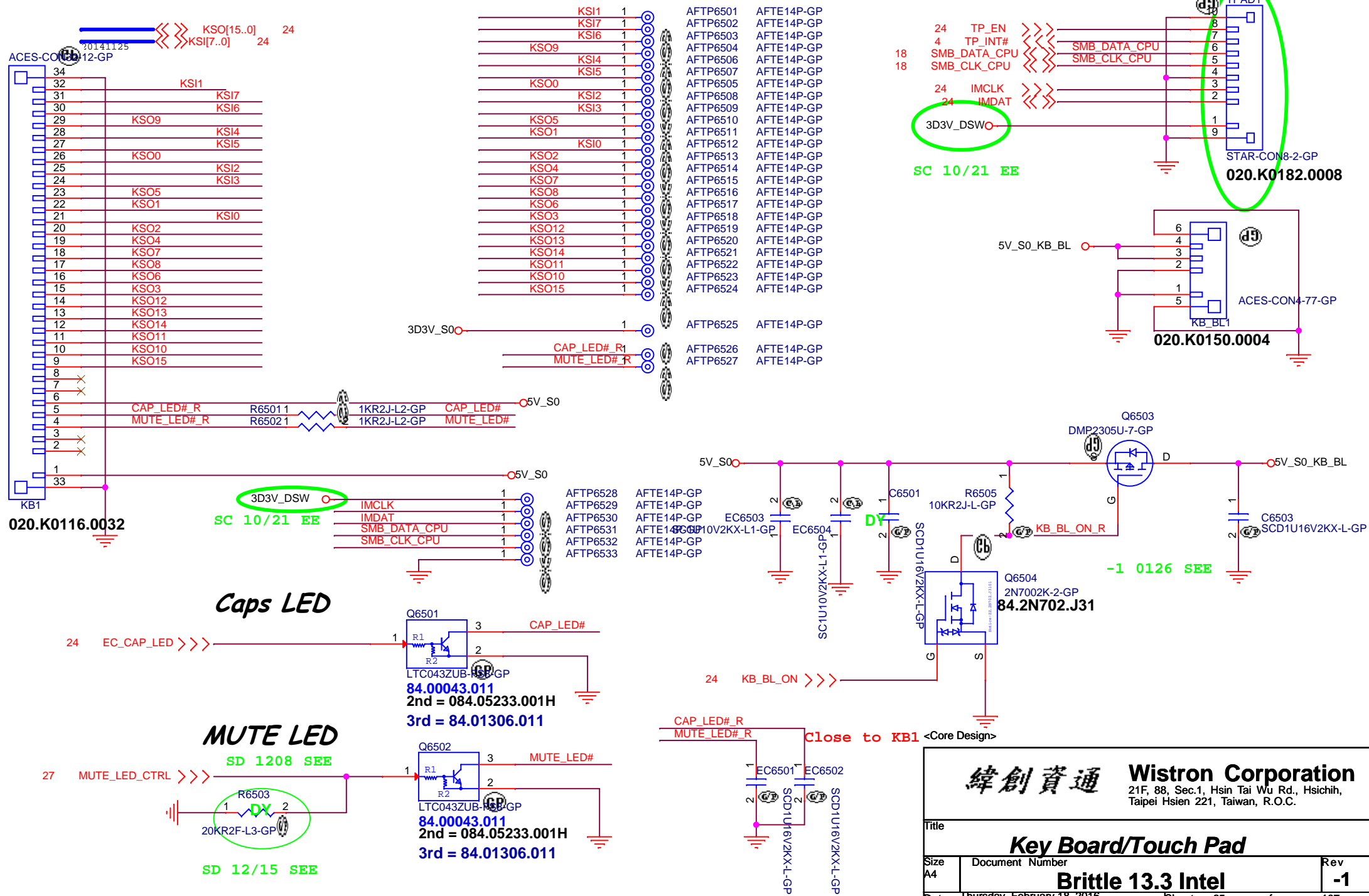
Rev	-1
-----	----

(Blanking)

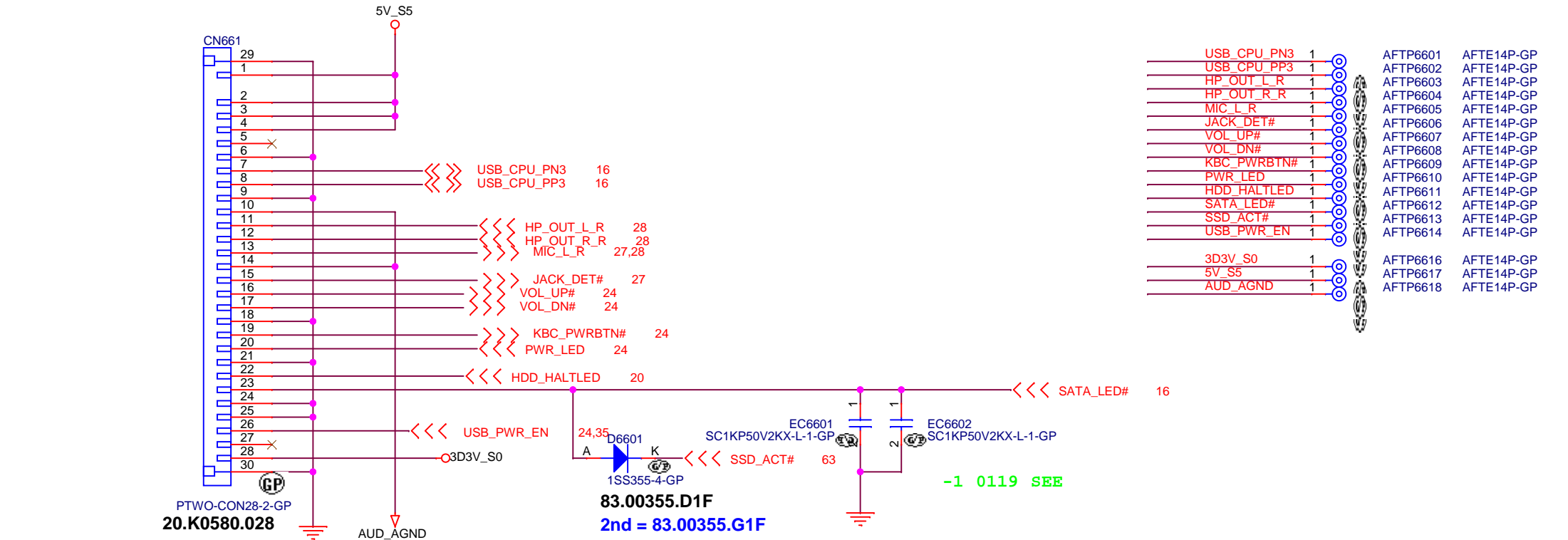
<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
LED Bard/Power Button		
Size	Document Number	Rev
A4	Brittle 13.3 Intel	
Date: Thursday, February 18, 2016		Sheet 64 of 107

SSID = Key Board CN & TP CN



IO Board Connector



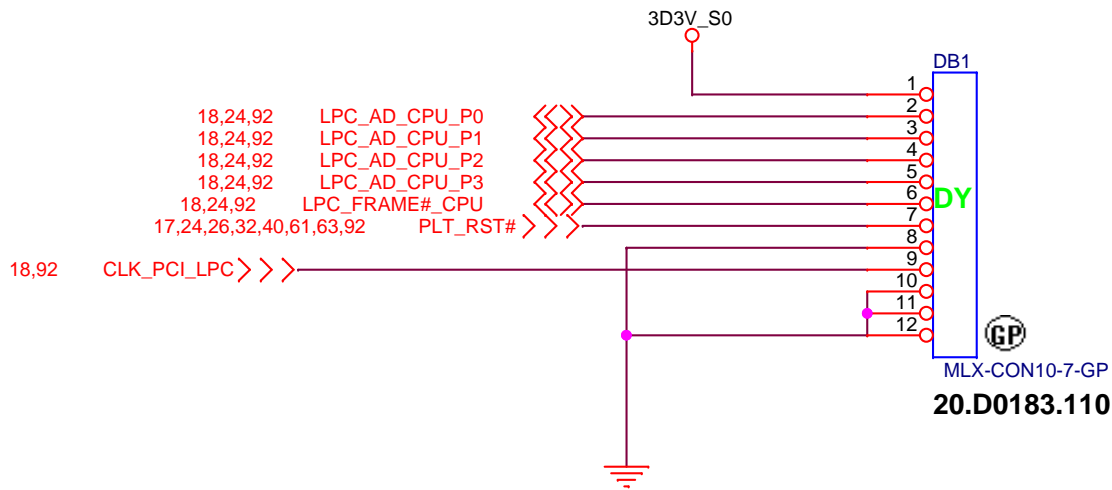
<Core Design>

緯創資通			Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
To IO Board Connector					
Size	Document Number				Rev
A4	Brittle 13.3 Intel				-1
Date:	Thursday, February 18, 2016		Sheet	66	of 107

(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Security Guard connector		
Size A	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016		Sheet 67 of 107

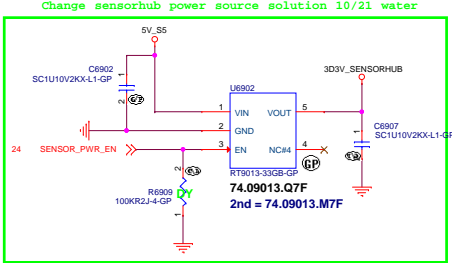
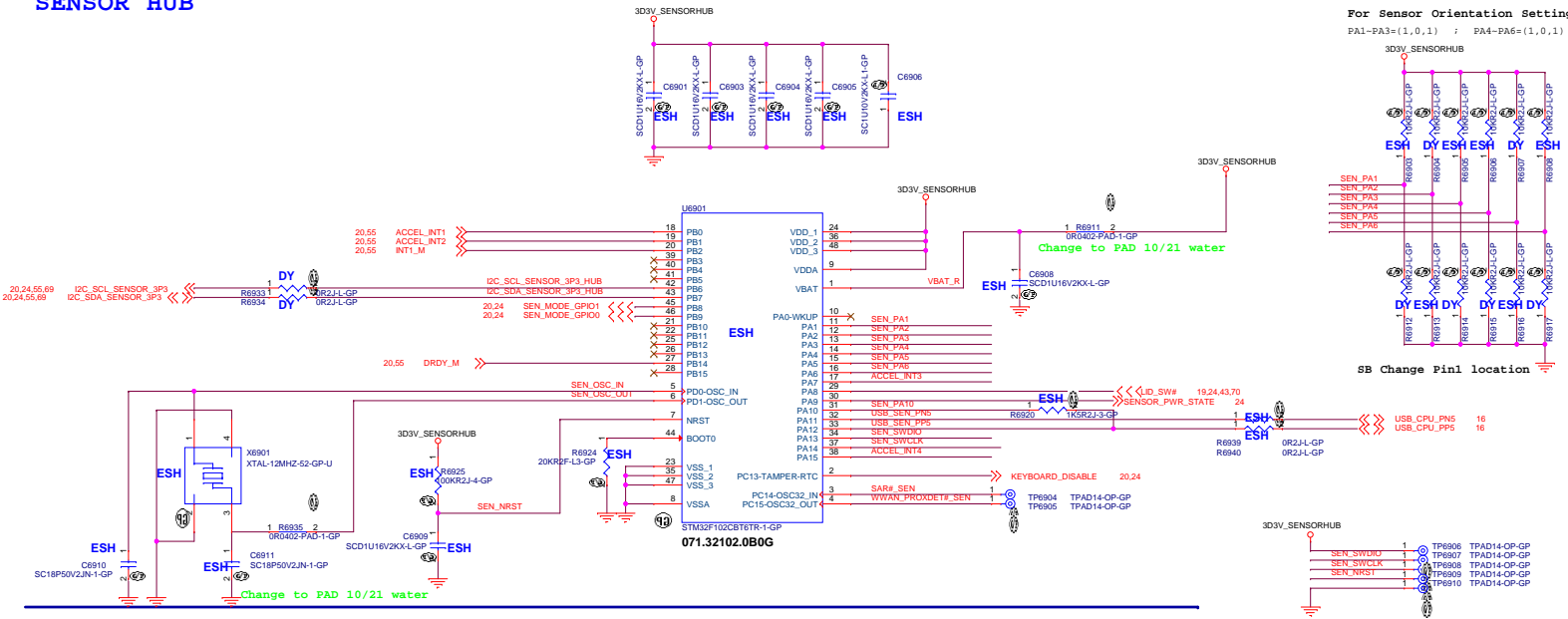


<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Dubug connector			
Size A	Document Number		Rev
	Brittle 13.3 Intel		-1
Date:	Thursday, February 18, 2016	Sheet 68 of 107	

Wistron Confidential document, Anyone can not create, Modify, Forward or any other pur application without get Wistron permission

SENSOR HUB



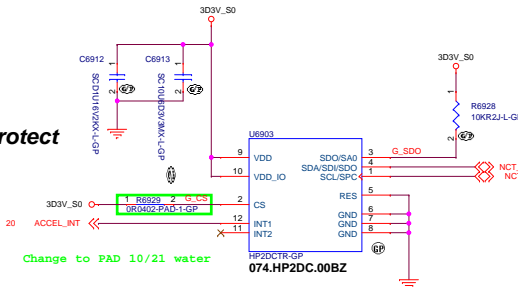
According to HP request for lid angle detect during S3 mode. We are need to add new GPIO from EC to MCU PA9 to inform sensorhub current status of OS. We may need to refer this signal for periodically wake up to detect lid angle during S3 state.

OS mode (Sensor hub Powered)	PA9 (Normal Low) from EC
S0	Low
S3	High

PB8	PB9	Mode
Low	Low	Laptop Mode (1)
Low	High	Stand Mode (2)
High	Low	Test Mode (3)
High	High	Tablet Mode (4)

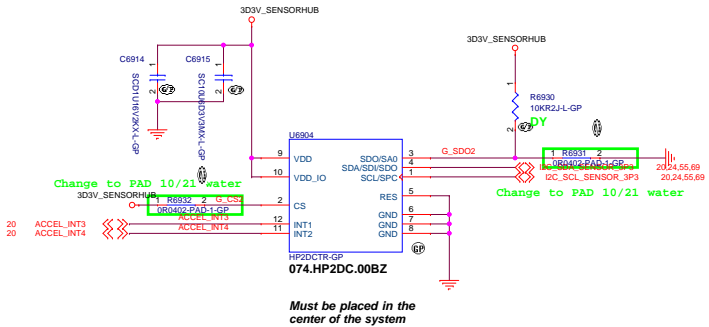
G-SENSOR

To KBC
for HDD Protect



To Sensor HUB
for LCD angle

Must be placed in the
center of the system



Must be placed in the
center of the system

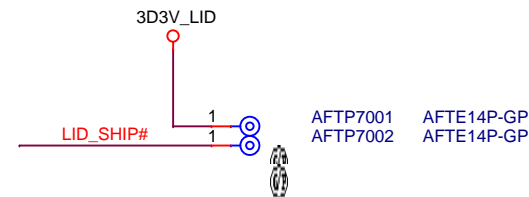
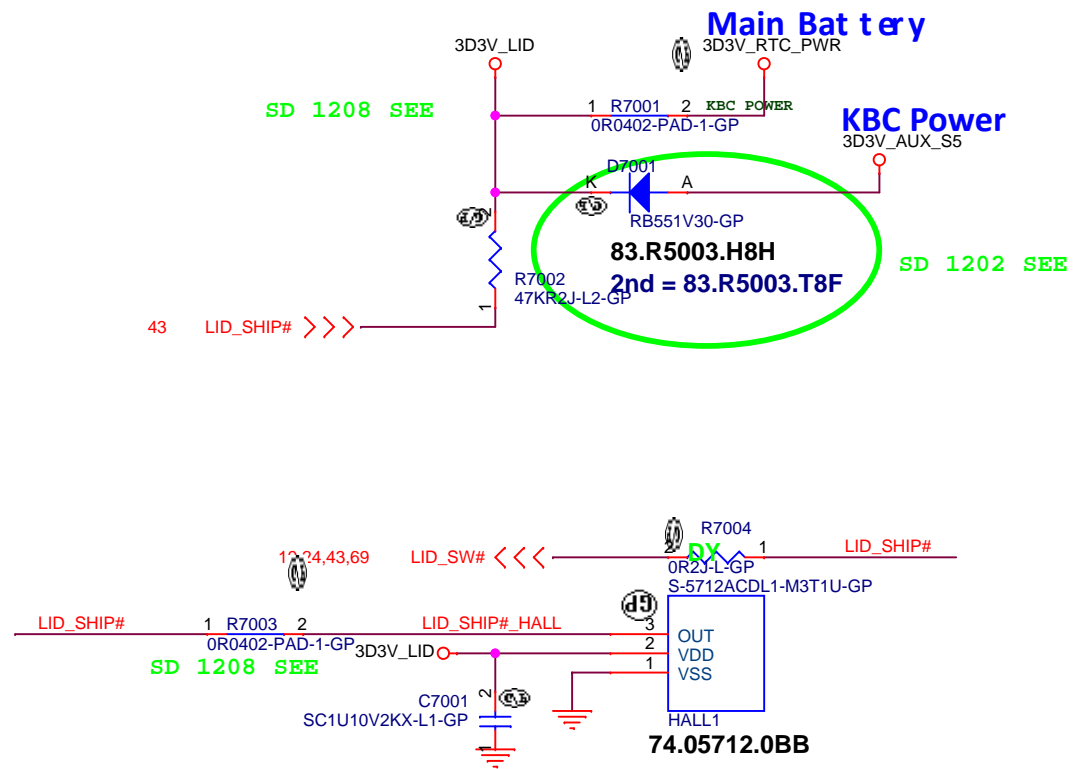
Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

Main Func = HALL SENSOR



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor/Vol Up,Down

Size
A4

Document Number

Brittle 13.3 Intel

Rev
-1

Date: Thursday, February 18, 2016

Sheet 70 of 107

(Blanking)

Wistron Confidential document, Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Thunderbolt (1/5)			
Size Custom	Document Number Brittle 13.3 Intel		Rev -1
Date: Thursday, February 18, 2016		Sheet 71 of	107

(Blanking)

Wistron Confidential document. Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

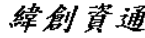
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thunderbolt (2/5)			
Size Custom	Document Number Brittle 13.3 Intel		Rev -1
Date: Thursday, February 18, 2016		Sheet 72 of	107

(Blanking)

Wistron Confidential document. Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thunderbolt (3/5)			
Size Custom	Document Number Brittle 13.3 Intel		Rev -1
Date: Thursday, February 18, 2016		Sheet 73 of	107

(Blanking)

Wistron Confidential document, Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thunderbolt (4/5)			
Size Custom	Document Number Brittle 13.3 Intel		Rev -1
Date: Thursday, February 18, 2016		Sheet 74 of	107

(Blanking)

Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title Thunderbolt (5/5)		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016		Sheet 75 of 107

(Blanking)

(Blanking)

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU DIGITALOUT (2/5)

Size
A3

Document Number
Brittle 13.3 Intel

Rev
-1

Date: Thursday, February 18, 2016

Sheet 77 of 107

(Blanking)

(Blanking)

(Blanking)

(Blanking)

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM1,2 (1/2)

Size
A3

Document Number

Rev
-1

Date: Thursday, February 18, 2016

Sheet 81 of 107

(Blanking)

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM3,4 (2/2)

Size
A3

Document Number

Rev
-1

Date: Thursday, February 18, 2016

Sheet 82 of 107


(Blanking)

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM1,2 (1/2)			
Size A4	Document Number Brittle 13.3 Intel		Rev -1
Date:	Thursday, February 18, 2016	Sheet 83 of	107

(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM1,2 (1/2)			
Size	Document Number		Rev
Custom	Brittle 13.3 Intel		-1
Date: Thursday, February 18, 2016		Sheet 84 of	107

(Blanking)

<Core Design>

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleVGA_CORE(RT8812AGQW)		
SizeA4	Document NumberBrittle 13.3 Intel	Rev-1
Date: Thursday, February 18, 2016		Sheet 85 of 107

(Blanking)

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title DISCRETE VGA POWER		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016		Sheet 86 of 107

(Blanking)

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DISCRETE VGA POWER

Size
A3

Document Number

Rev
-1

Date: Thursday, February 18, 2016

Sheet 87 of 107

(Blanking)

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

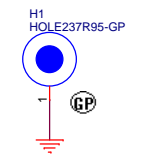
Document Number
Brittle 13.3 Intel

Rev
-1

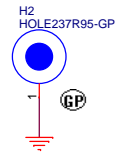
Date: Thursday, February 18, 2016

Sheet 88 of 107

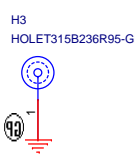
ZZ.00PAD.921



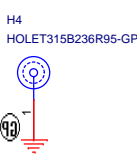
ZZ.00PAD.921



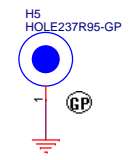
ZZ.00PAD.931



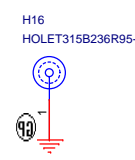
ZZ.00PAD.931



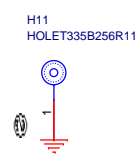
ZZ.00PAD.921



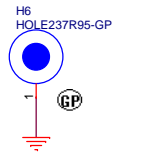
ZZ.00PAD.931



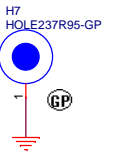
ZZ.00PAD.D21



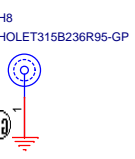
ZZ.00PAD.921



ZZ.00PAD.921

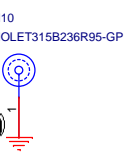


ZZ.00PAD.931

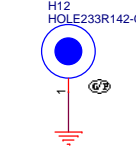


SD 1201 SEE

ZZ.00PAD.931



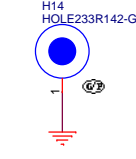
ZZ.00PAD.5S1



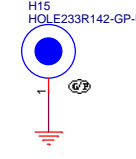
ZZ.00PAD.5S1



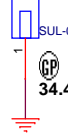
ZZ.00PAD.5S1



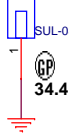
ZZ.00PAD.5S1



SCG1



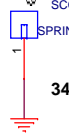
SCG2



SCG3



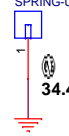
SCG4



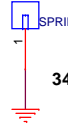
SCG5



SPR1



SCG6



SCG7



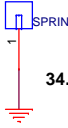
SCG8



SCG9



SCG10



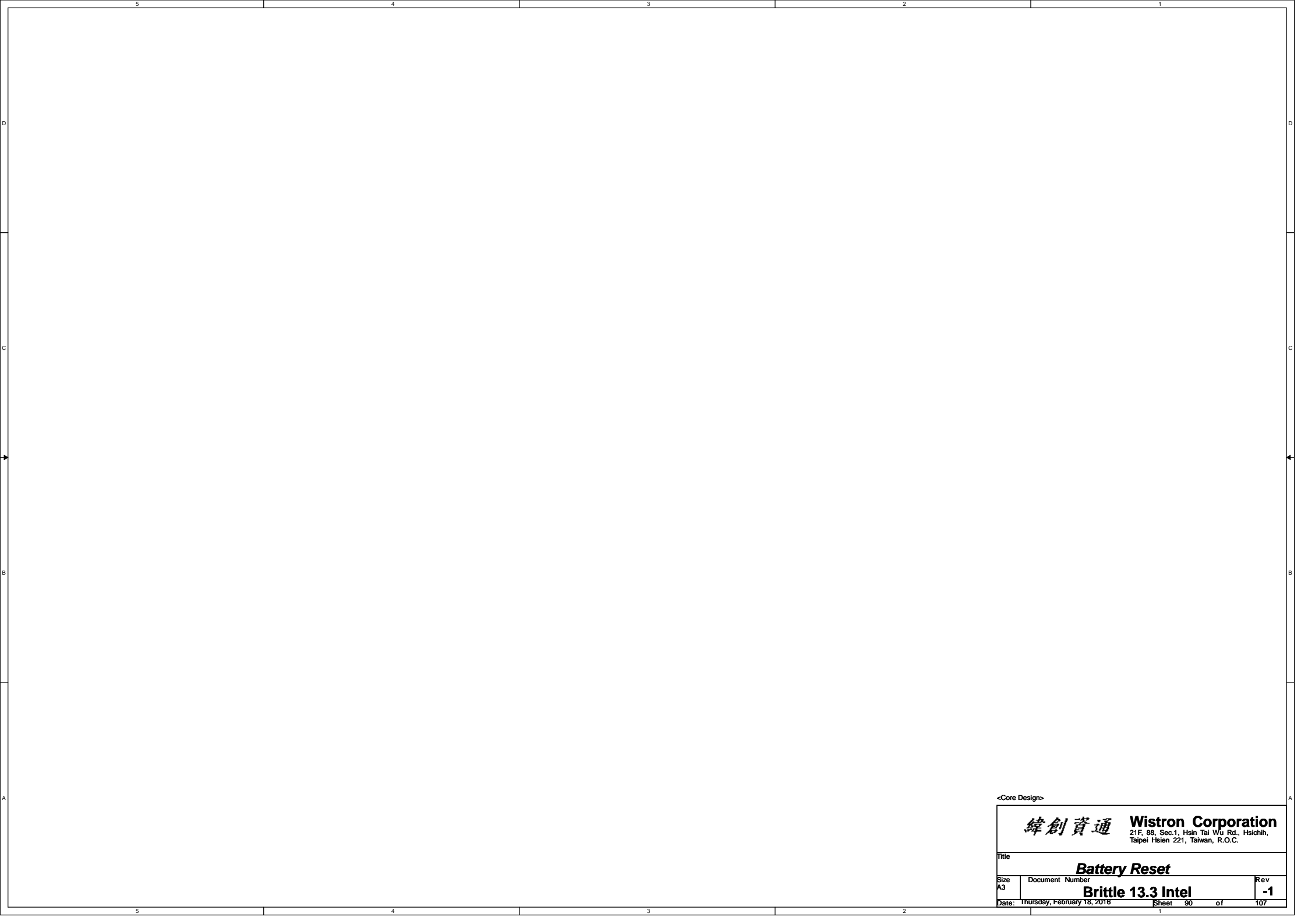
SCG11



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

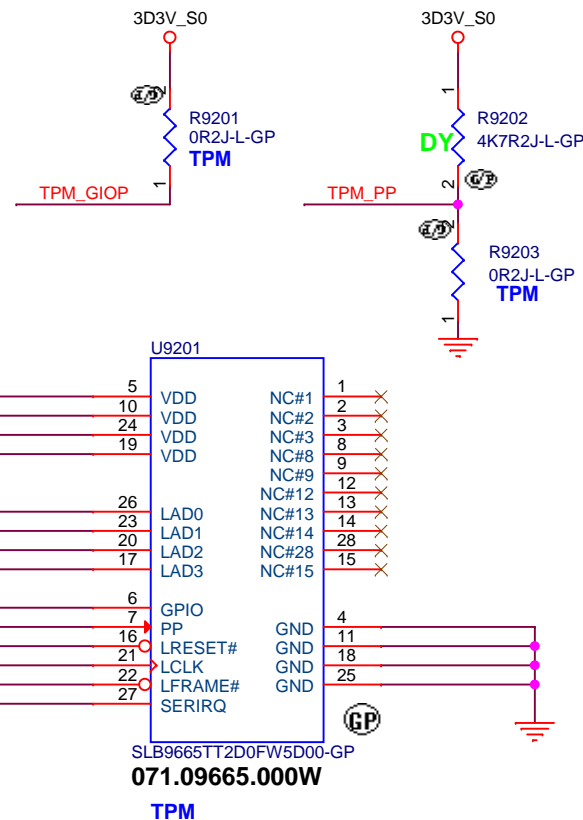
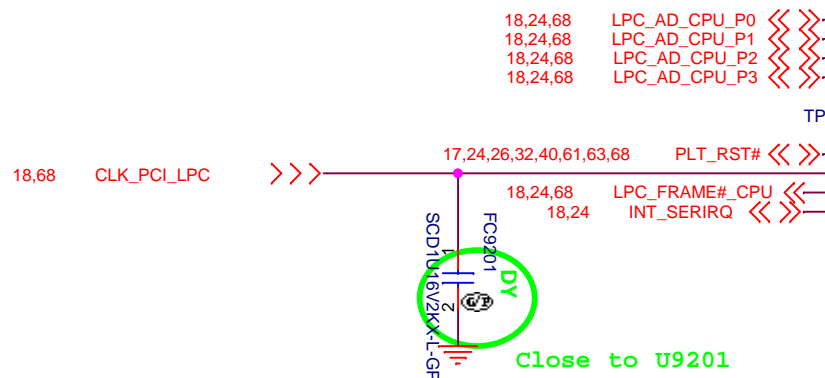
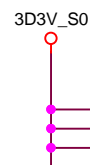
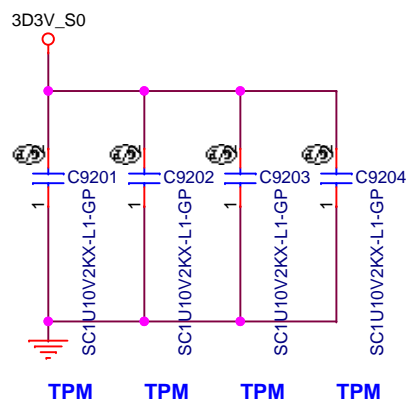
Title			UNUSED PARTS/EMI Capacitors
Size	Document Number	Rev	
A3		-1	
Date:	Thursday, February 18, 2016	Sheet	89 of 107



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Battery Reset			
Size	Document Number		Rev
A3	Brittle 13.3 Intel		-1
Date:	Thursday, February 18, 2016		
	Sheet	90 of	107

(Blanking)



Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission
<Core Design>

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title TPM</p>		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016	Sheet 92 of 107	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A	Document Number Brittle 13.3 Intel		Rev -1
Date:	Thursday, February 18, 2016	Sheet 93 of	107

	A	B	C	D	E
4					
3					
2					
1					

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Brittle 13.3 Intel		Rev -1
Date:	Thursday, February 18, 2016	Sheet 94 of 107	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A	Document Number Brittle 13.3 Intel		Rev -1
Date:	Thursday, February 18, 2016	Sheet 95 of	107

PCH_XDP 26Pin Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH_XDP

Size

Project Name

Rev

Date: Thursday, February 18, 2016

Sheet 98 of 107

Brittle 13.3 Intel
-1

A

B

C

D

E

4

3

2

1

Wistron Confidential document, Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
table of content			
Size	Document Number		Rev
A3	Brittle 13.3 Intel		-1
Date:	Thursday, February 18, 2016	Sheet 97 of	107

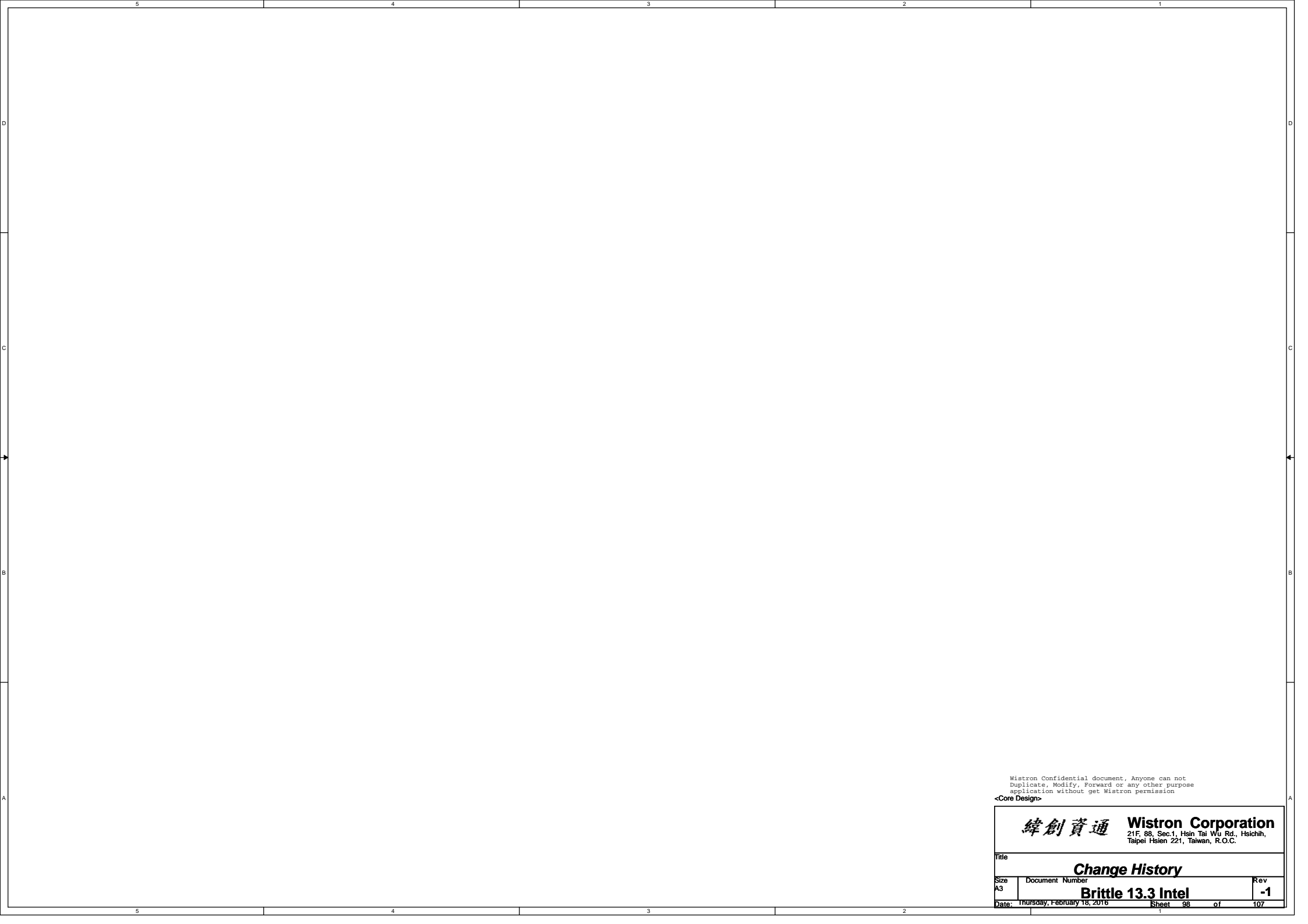
A

B

C

D

E



Wistron Confidential document, Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

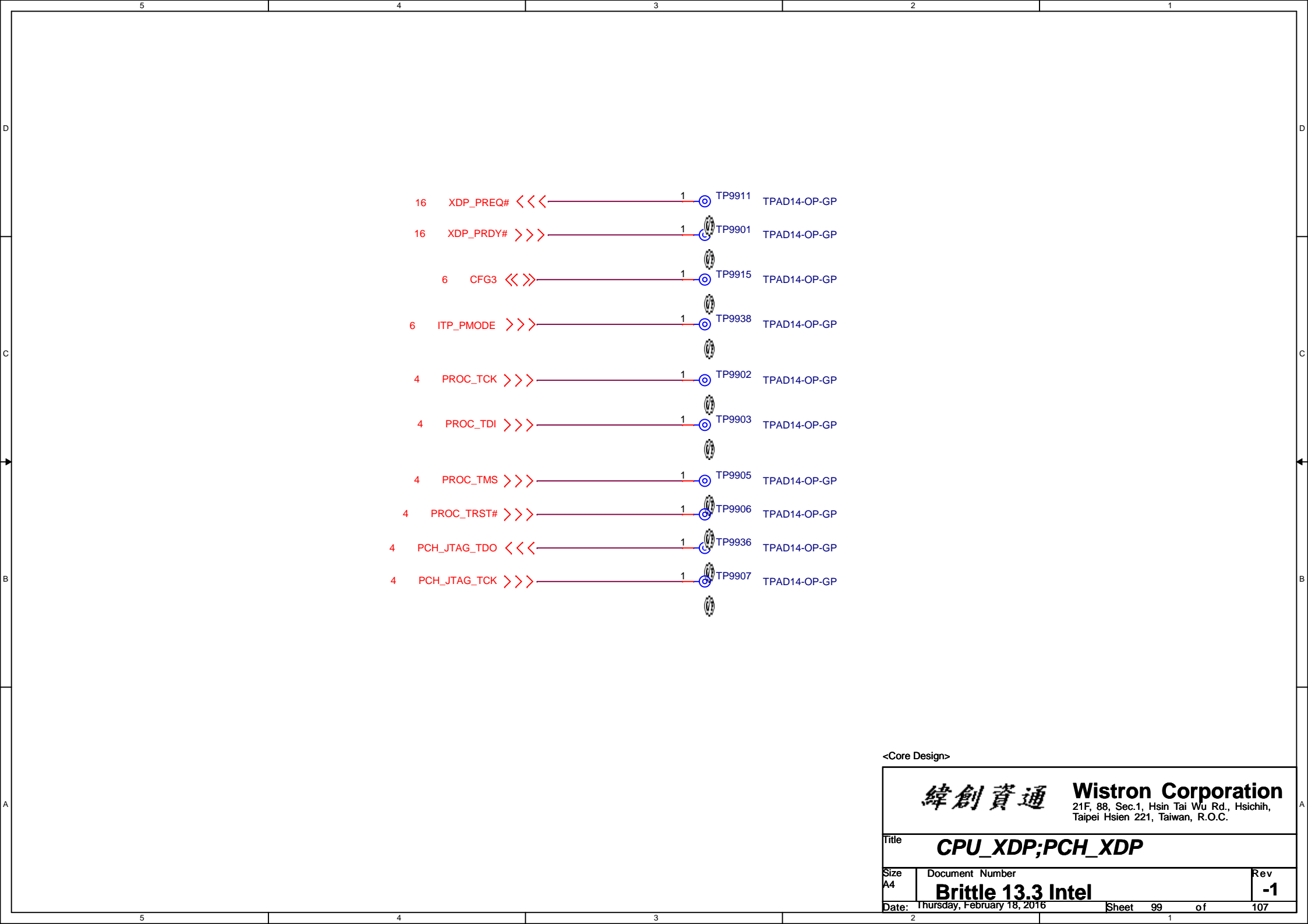
Size
A3

Document Number

Rev
-1

Date: Thursday, February 18, 2016

Sheet 98 of 107



<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title CPU_XDP;PCH_XDP		
Size A4	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016		Sheet 99 of 107

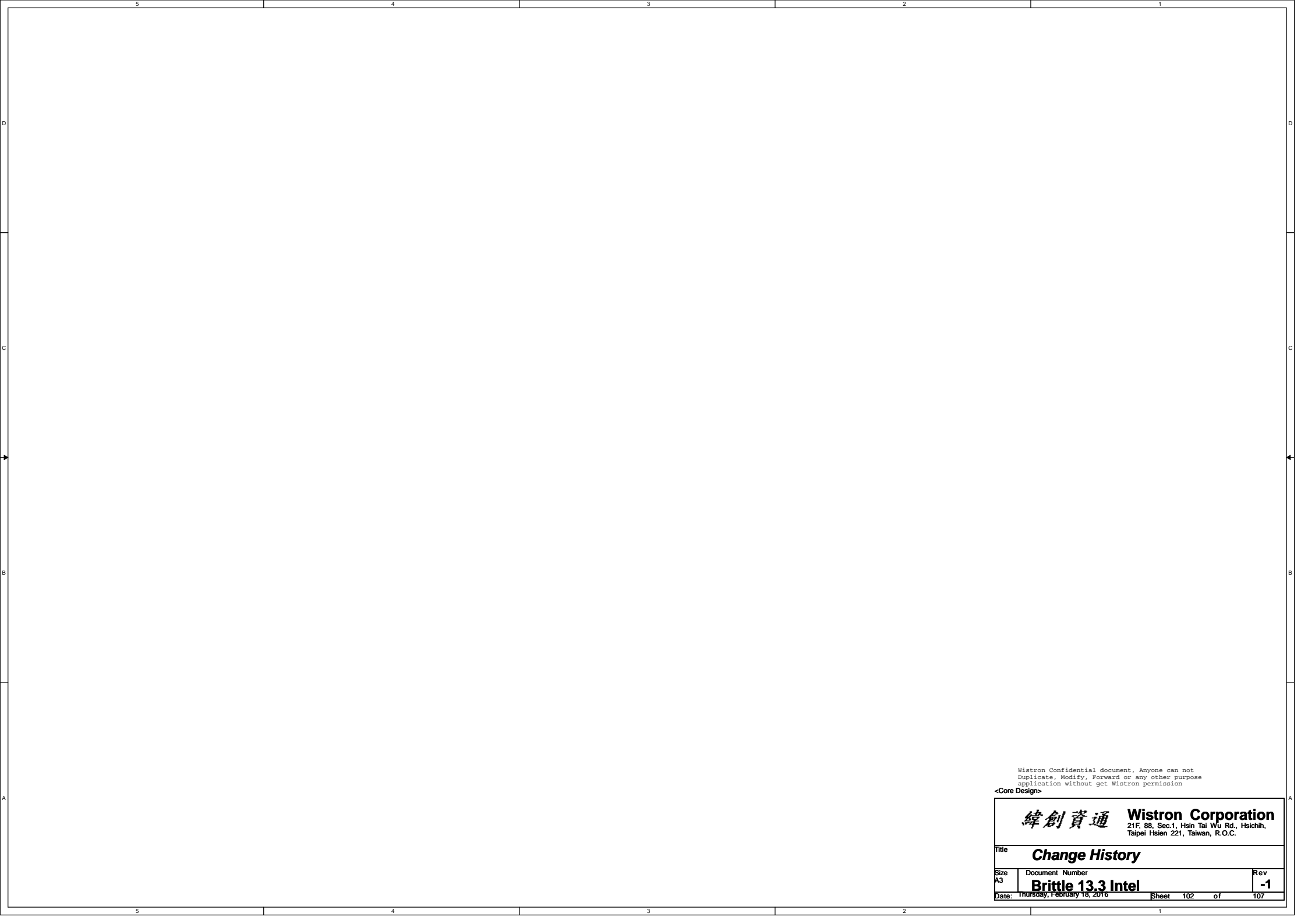
5	4	3	2	1
D				
C				
B				
A				

Wistron Confidential document, Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power Sequence			
Size A3	Document Number		Rev -1
Brittle 13.3 Intel			
Date:	Thursday, February 18, 2016	Sheet 100 of	107





Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title Change History		
Size A3	Document Number Brittle 13.3 Intel	Rev -1
Date: Thursday, February 18, 2016		Sheet 102 of 107

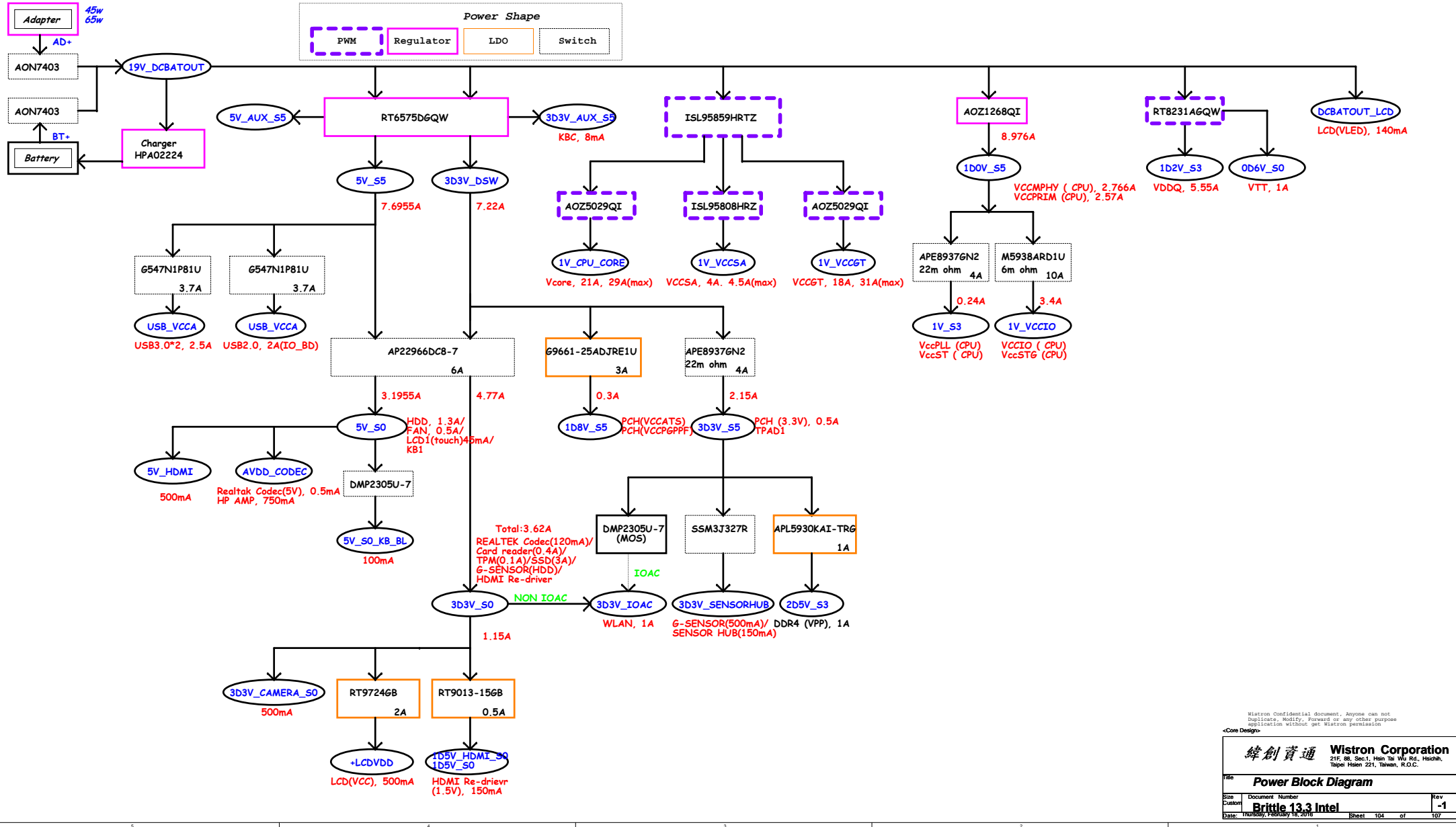
BRITTLE POWER UP SEQUENCE DIAGRAM

Timing diagram for the 74VHC04 inverter. The diagram shows the relationship between the input signal (IN_A3) and the output signal (OUT_Y0). The input signal is a square wave with a period of 10ns. The output signal is an inverted square wave with a period of 10ns. The propagation delay is approximately 1.5ns. The output signal is labeled as 'OUT_Y0' and the input signal is labeled as 'IN_A3'. The output signal is also labeled as 'OUT_Y0' and the input signal is labeled as 'IN_A3'. The output signal is also labeled as 'OUT_Y0' and the input signal is labeled as 'IN_A3'.

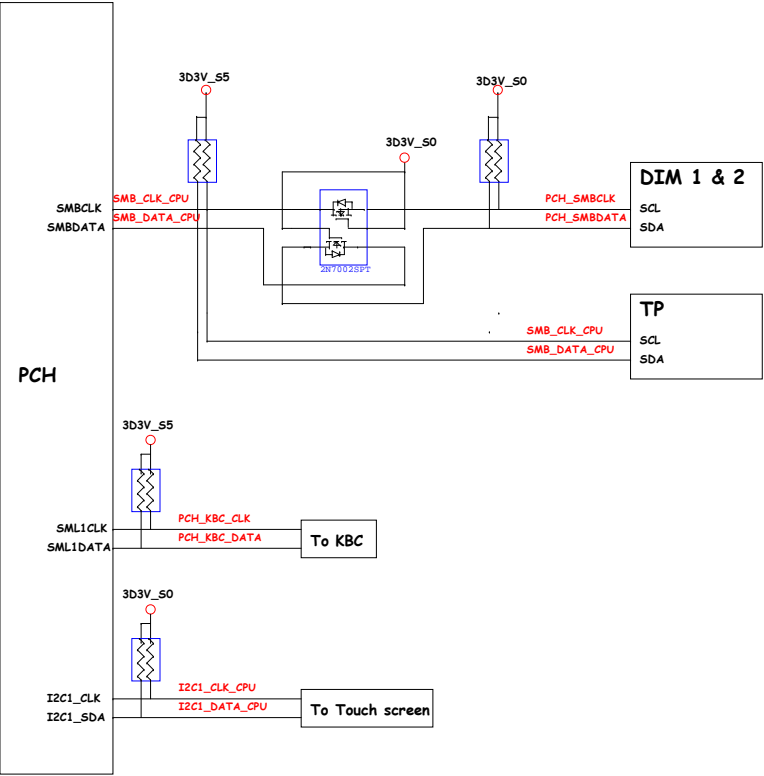
#544924 END P.123

Name	Source	Destination	Description
LAN_WAKE#	PHY	PCB	Can be used by the LAN PHY as a wake signal.
ESPI_RESET#	PCB	Platform	Controls reset to eSPI
VCCST_PWRGD	Platform	Processor	Indication that the VCCST1VDDQ power supplies are stable and within specification
DDR_VTT_CM#	CPU	VTT VR	Enable signal for the DDR VTT VR
SLEEP_S0#	PCB	Platform	S0 Sleep Control. When PC1 is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

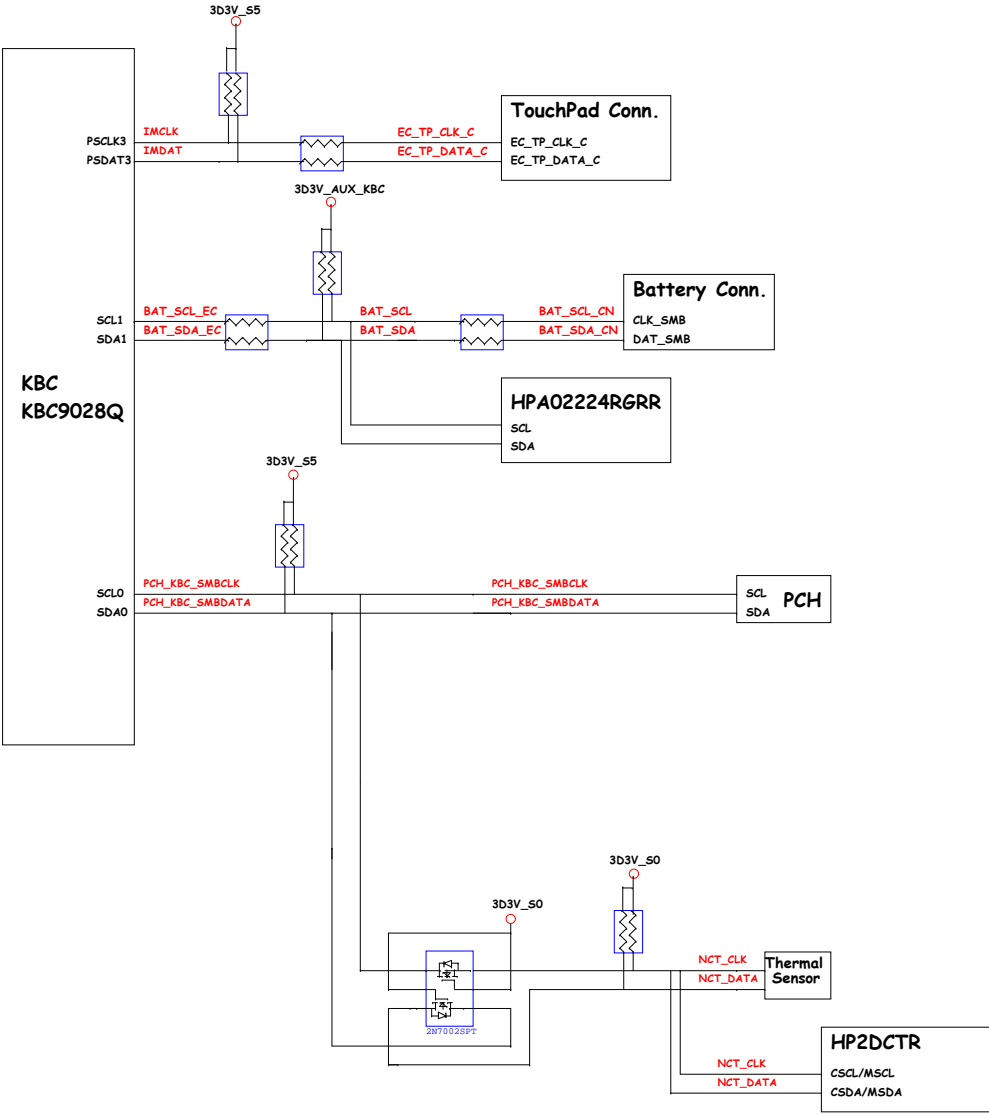
OPCE_RCOMP	<p>On Package Cache resistance Compensation from OPC: Refer to the appropriate platform design guide for implementation details values. Unconnected for Processors without OPC.</p> <p>System Memory Power Gate Control: When signal is high - platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C3s and deeper and S3.</p>	N/A	A	SE	U/H-Processor lines with On Package Cache
SGR_VTT_CTRL		0	CHDS	SE	All processor lines



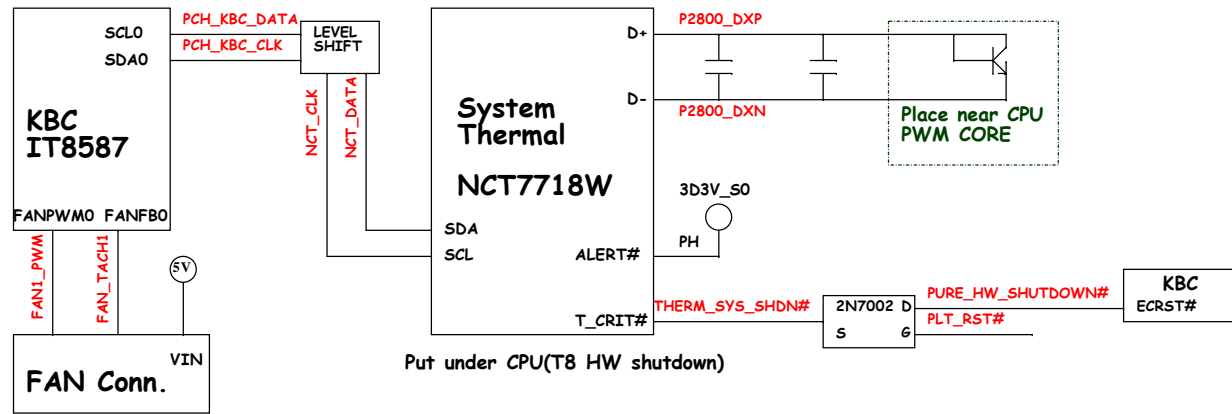
PCH SMBus Block Diagram



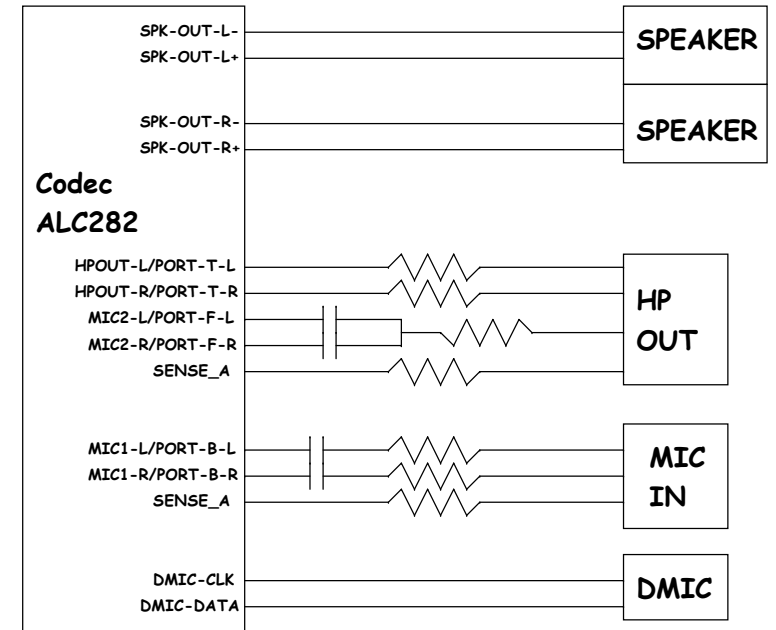
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Wistron Confidential document. Anyone can not
Duplicate, Modify, Forward or any other purpose
application without get Wistron permission

<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title THERMAL/AUDIO BLOCK DIAGRAM			
Size Custom	Document Number Brittle 13.3 Intel	Rev -1	
Date: Thursday, February 18, 2016	Sheet 106	of	107

